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UNITED STATES DISTRICT COURT  
NORTHERN DISTRICT OF CALIFORNIA  
SAN JOSE DIVISION

IN RE INTEL CORP. SECURITIES  
LITIGATION

) Case No. 5:20-cv-05194-EJD

) (Consolidated)

) CLASS ACTION

) CONSOLIDATED CLASS ACTION  
) COMPLAINT FOR VIOLATIONS OF THE  
) FEDERAL SECURITIES LAWS

) Jury Trial Demanded

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## ABBREVIATIONS & DEFINITIONS

AMD .....	Advanced Micro Devices, Inc.
ARM .....	ARM Holdings, Ltd.
ASML .....	ASML Holding N.V.
ASP .....	Average Selling Price
Cannon Lake .....	Intel's 10 nm chip microarchitecture
Cascade Lake .....	Intel's 14 nm chip microarchitecture
CCG .....	Intel's Client Computing Group
CEO.....	Chief Executive Officer
CFO.....	Chief Financial Officer
CPU.....	Central Processing Unit
DCG .....	Intel's Data Center Group
Diamond Rapids.....	Intel's 7 nm chip microarchitecture
DOE .....	U.S. Department of Energy
EUV .....	Extreme Ultraviolet Lithography
GPGPU .....	General Purpose Graphics Processing Unit
GPU.....	Graphics Processing Unit
Granite Rapids .....	Intel's 7 nm chip microarchitecture
HPC.....	High Performance Computing
Ice Lake.....	Intel's 10 nm chip microarchitecture
IDM.....	Integrated Device Manufacturer
IOTG .....	Internet of Things Group
nm .....	nanometer
NSG.....	Non-Volatile Memory Solutions Group
Nvidia.....	Nvidia Corporation
ODM .....	Original Design Manufacturer
OEM.....	Original Equipment Manufacturer
PAO.....	Process-Architecture-Optimization

1 PC..... Personal Computer  
2 Ponte Vecchio .....Intel’s 7 nm GPGPU  
3 PSG .....Intel’s Programmable Solutions Group  
4 Samsung.....Samsung Foundry  
5 Sapphire Rapids .....Intel’s 14 nm chip microarchitecture  
6 Tiger Lake .....Intel’s 10 nm chip microarchitecture  
7 TMG.....Intel’s Technology and Manufacturing Group  
8 TSCG .....Intel’s Technology, Systems Architecture and Client Group  
9 TSMC.....Taiwan Semiconductor Manufacturing Company Ltd  
10 Xeon® ..... Intel’s product line of server CPUs

1 Court-appointed Lead Plaintiffs KBC Asset Management NV (“KBC”) and SEB Investment  
2 Management AB (“SEB,” and together, “Lead Plaintiffs”), individually and on behalf of a class of  
3 similarly situated persons and entities, by their undersigned attorneys, allege the following against Intel  
4 Corporation (“Intel” or the “Company”) and the Individual Defendants (defined below), upon personal  
5 knowledge as to themselves and their own acts, and upon information and belief as to all other matters.

6 Lead Plaintiffs bring this federal securities class action on behalf of themselves and a class  
7 consisting of all persons and entities who purchased, or otherwise acquired, Intel common stock from  
8 October 25, 2019 through October 23, 2020, inclusive (the “Class Period”), and who were damaged  
9 thereby, subject to certain exclusions addressed in paragraph 228 below (the “Class”). The Defendants  
10 in this action are: Intel; Robert (Bob) H. Swan (“Swan”), Intel’s Chief Executive Officer (“CEO”);  
11 Dr. Venkata S.M. (Murthy) Renduchintala (“Renduchintala”), Intel’s former Chief Engineering Officer  
12 and President of the Company’s Technology, Systems Architecture and Client Group; and George S.  
13 Davis, Intel’s Chief Financial Officer (“CFO”). Lead Plaintiffs’ and the Class’s claims arise under  
14 Sections 10(b) and 20(a) of the Securities Exchange Act of 1934 (“Exchange Act”) and Rule 10b-5  
15 promulgated thereunder.

16 Lead Plaintiffs’ allegations concerning matters other than themselves and their own acts are based  
17 upon the investigation conducted by and through counsel, which included, among other things, the review  
18 and analysis of: (i) transcripts, press releases, news articles, and other public statements issued by or  
19 concerning Intel and the Individual Defendants; (ii) research reports issued by financial and industry  
20 analysts concerning the Company; (iii) reports and other documents filed publicly by Intel with the U.S.  
21 Securities and Exchange Commission (“SEC”); (iv) Intel’s corporate website; (v) interviews with former  
22 employees of the Company; (vi) media reports about the Company; and (vii) other publicly available  
23 information. Lead Plaintiffs’ investigation continues. Lead Plaintiffs believe that substantial additional  
24 evidentiary support will exist for the allegations set forth below after a reasonable opportunity for  
25 discovery.

## 26 **I. INTRODUCTION**

27 1. Lead Plaintiffs’ claims arise from Defendants’ materially false and misleading statements  
28 and omissions regarding the status of Intel’s 7 nanometer (“nm”) chipmaking process and the continued

1 viability of the Company's business model of manufacturing its most advanced chips in-house as an  
2 integrated device manufacturer ("IDM"). Since the late 1990s, Intel had established a commanding lead  
3 over its competitors in microprocessor development and production, which secured the Company's  
4 dominant position in the semiconductor industry. Intel's competitive advantage over its industry peers  
5 has historically stemmed directly from its IDM business model, pursuant to which Intel both designed  
6 *and* manufactured (in-house) each successive generation of increasingly smaller-scale chips (i.e., 14 nm,  
7 10 nm, 7 nm, etc.). Intel's IDM model was key to its ability to create industry-leading microprocessors,  
8 and to its impressive profitability, as it could produce chips in-house for lower costs than its competitors,  
9 who outsource manufacturing to third-party chipmaking facilities known as "foundries."

10 2. Recently, however, Intel has suffered numerous setbacks to this critical aspect of its  
11 business. Difficulties in Intel's manufacturing process have resulted in repeated delays, starting with the  
12 rollout of its 14 nm process, and continuing more prominently with its more recent 10 nm process, and  
13 have eroded Intel's long-held industry leadership. As Intel faced these increasing chipmaking challenges,  
14 Intel's competitors began methodically closing the technology gap, ultimately bringing more advanced,  
15 smaller-scale chip technology to market sooner than Intel. Thus, Intel's delays in rolling out its leading-  
16 edge chips imperiled its leading position in the industry and cost the Company significant market share.  
17 These delays also raised concerns from investors about whether Intel could continue manufacturing its  
18 most advanced chips in-house under its IDM model, which Intel has described as "foundational to our  
19 current and future success."

20 3. Against this backdrop, Intel sought to reassure the market that it was on track with its  
21 next-generation 7 nm process development. The successful rollout of the 7 nm process would allow the  
22 Company to retake its leadership role in new chip technology, defend its market share against the  
23 encroachment by its competitors, and reaffirm that its IDM business model was viable and would  
24 continue to provide the Company with advantages over its competitors. The timely development and  
25 ramp-up of Intel's 7 nm capabilities, and the continued viability of its purported IDM advantage, were  
26 therefore critically important to the Company, its investors, and the value of its stock.

27 4. Thus, throughout the Class Period, Defendants repeatedly assured the market that Intel  
28 had learned from its past difficulties with the 10 nm process, and was "on track" to launch its flagship

1 7 nm product in 2021, which was a “halo” product called “Ponte Vecchio” intended for a high-profile  
2 U.S. Department of Energy (“DOE”) supercomputer. Defendants further assured investors that Intel’s  
3 production of critical 7 nm server CPU chips would “follow[] shortly after in 2022.” Intel also continued  
4 to emphasize that its “in-house manufacturing” remained “an important advantage” over its competitors.

5 5. As set forth more fully herein, these and similar statements were false or misleading when  
6 made. In reality, Defendants knew or recklessly disregarded that Intel’s 7 nm process was suffering from  
7 technological setbacks that would render it impossible for Intel to meet the publicly disclosed 2021  
8 timeline for its next-generation 7 nm Ponte Vecchio chip and 2022 timeline for its 7 nm server CPUs.  
9 Indeed, by no later than December 2019, Intel’s own internal product roadmaps showed that the  
10 development of its 7 nm process was already at least one year behind the publicly announced schedule.  
11 Consistent with this fact, in March 2020, Intel missed a critical “hard tapeout” deadline for the Ponte  
12 Vecchio product, rendering it essentially impossible for Intel to meet the deadline for that product and  
13 the additional products that were supposed to launch quickly thereafter. In May 2020, another internal  
14 Intel product roadmap re-confirmed that Intel was at least one year behind the publicly stated timeline  
15 for its 7 nm server CPU products. Yet, throughout this entire time, including up through June 2020,  
16 Defendants continued to falsely reassure investors that Intel was “on track” to meet its publicly stated  
17 launch dates, when in fact the Company was woefully behind schedule.

18 6. On July 23, 2020, just weeks after most recently reassuring investors that Intel was on  
19 track to meet its deadlines, Defendants flatly reversed course. That day, Defendants revealed that Intel  
20 was not at all “on track” for a timely launch of its 7 nm chips but was instead twelve months behind  
21 schedule due to a “defect” resulting in “yield degradation.” Defendants further admitted that the  
22 manufacturing of Intel’s first 7 nm product, Ponte Vecchio, would be outsourced to a competitor, and  
23 that its high-margin 7 nm server CPU chips would not be available until “the first half of [2023].” The  
24 July 2020 announcement marked the first time in Intel’s history that the Company was forced to outsource  
25 production of one of its cutting-edge microprocessor designs to a competitor. The extended delay  
26 indicated that fundamental technical issues remained to be solved. These announcements cast grave  
27 doubts on the health and feasibility of Intel’s 7 nm product and its IDM business model, into which the  
28 Company had invested tens of billions of dollars in recent years.



1           7.       The market response was immediate and overwhelmingly negative. For example, on  
2 July 24, 2020, Sanford C. Bernstein & Co. (“Bernstein”) analysts published a report stating that Intel’s  
3 Q2 earnings call was “the worst we have seen in our career covering the company” and that Intel’s  
4 management had suffered “a complete loss of credibility.” The analysts observed that “[f]rom here we  
5 see things growing increasingly painful as 7nm delays are likely to overshadow anything good they [Intel]  
6 can put forth, while magnifying any negative events, all while they fight an existential conflict with  
7 themselves as they attempt to figure a way out of the hole they have dug. . . . While Intel suggested they  
8 at least know what the problem is, it certainly doesn’t sound like a fix is forthcoming anytime soon given  
9 the magnitude of the delay and Intel’s potential solution, namely, to possibly give up and embrace a much  
10 larger outsourcing strategy.” The report stated “we are back to square one, with Intel’s process  
11 deficiencies now growing wider than ever,” and added “any shreds of credibility this management team  
12 might have had have now gone out the window.”

13           8.       Others were equally stunned. Analysts at Susquehanna Financial Group, LLLP  
14 (“Susquehanna”) called the revelations a “dropped bomb,” *Bloomberg* reported that “the worst fear[]  
15 over Intel’s pipeline is now realized,” and *ExtremeTech* stated Intel’s about-face was “historically  
16 unprecedented.”

17           9.       The impact on Intel’s investors was swift and devastating. Intel stock price declined by  
18 \$10.83 per share, or **17.93%**, from a closing price of \$60.40 per share on July 23, 2020, to a closing price  
19 of \$49.57 per share on July 27, 2020. On July 27, 2020, as a result of the 7 nm delays, Defendant  
20 Renduchintala, who directly oversaw Intel’s development of the 7 nm process, resigned from Intel  
21 abruptly, effective August 3, 2020.

22           10.      On October 22, 2020, Defendants issued another round of crushing disclosures. That day,  
23 they confirmed that Intel’s Ponte Vecchio was not the only 7 nm chip that the Company was considering  
24 outsourcing, and in fact this “contingency plan” could also apply to Intel’s 7 nm server CPU chips – a  
25 tacit admission that Intel’s IDM advantage had evaporated for the Company’s most critical products.

26           11.      Analysts again reacted with surprise and disappointment. For example, the following day,  
27 Bernstein lowered its price target to \$40 (from \$45) in a report entitled “Don’t think it can’t get  
28 worse . . .” which stated that “[w]hile we thought [the July 2020] call was bad, last night’s was

1 potentially even worse as fundamentals are now deteriorating at an alarming pace . . . .” With respect to  
2 Intel’s advanced node production, the analysts “struggle[d] with how the company can have any  
3 confidence on achieving 2023 ‘product leadership’ on 7nm (as right now they have no idea what they  
4 will be shipping, nor do their customers).” Other analysts also took note of Swan’s expanded comments  
5 about outsourcing cutting-edge CPU manufacturing to external foundries, and the harsh implications for  
6 Intel’s IDM business model. On this point, Jefferies noted that Intel’s “CEO commentary has gone from  
7 ‘we continue to look at . . . non-CPU products in foundries’ in January, to ‘our 2023 products will deliver  
8 on either Intel 7nm or external foundry processes’ during its Oct ‘20 earnings call.”

9 12. These disclosures caused the price of Intel stock to decline by another **10.57%**, or \$5.70  
10 per share, from a closing price of \$53.90 per share on October 22, 2020, to a closing price of \$48.20 per  
11 share on October 23, 2020.

12 13. On January 13, 2021, as a direct consequence of Intel’s floundering development of the  
13 7 nm, the Intel Board ousted Swan and announced that he would be departing the Company on  
14 February 15, 2021. After this announcement, Intel’s stock price surged. Meanwhile, industry analysts  
15 continued to observe that Defendants misled the investing public concerning the matters alleged herein.  
16 For instance, on January 11, 2021, widely respected industry news source SemiAccurate reported: “Intel  
17 management has repeatedly downplayed crippling problems and has more skeletons in the closet than  
18 anyone understands. Every time an opportunity presents itself to come clean, management does the  
19 opposite . . . .”

## 20 **II. JURISDICTION AND VENUE**

21 14. The claims asserted herein arise under and pursuant to §§ 10(b) and 20(a) of the Exchange  
22 Act, 15 U.S.C. §§ 78j(b) and 78t(a), and Rule 10b-5 promulgated thereunder by the SEC, 17 C.F.R.  
23 § 240.10b-5. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C.  
24 § 1331 and § 27 of the Exchange Act.

25 15. Venue is proper in this District pursuant to § 27 of the Exchange Act and 28 U.S.C.  
26 § 1391(b). Many of the acts charged herein, including the preparation and dissemination of materially  
27 false and misleading information, occurred in substantial part in this District.  
28

1           16. In connection with the acts alleged in this complaint, Defendants, directly or indirectly,  
2 used the means and instrumentalities of interstate commerce, including, but not limited to, the mails,  
3 interstate telephone communications and the facilities of the NASDAQ stock exchange (“NASDAQ”).

### 4 **III. THE PARTIES**

#### 5 **A. Lead Plaintiffs**

6           17. On October 20, 2020, this Court appointed KBC and SEB to serve as Lead Plaintiffs in  
7 this action pursuant to the Private Securities Litigation Reform Act of 1995 (the “PSLRA”).

8           18. KBC is a wholly owned subsidiary and asset management arm of KBC Bank NV, a  
9 multinational financial company headquartered in Brussels, Belgium. As part of KBC’s asset  
10 management services, it is responsible for managing mutual funds, private funds, and institutional funds.  
11 KBC manages assets in excess of €100 billion. As set forth in its PSLRA certification, KBC’s funds  
12 purchased Intel common stock during the Class Period and suffered damages as a result of the securities  
13 law violations alleged herein.

14           19. SEB is a subsidiary of Skandinaviska Enskilda Banken AB and part of the SEB Group.  
15 SEB manages more than €100 billion for institutional and private investors. As set forth in its PSLRA  
16 certification, SEB purchased Intel common stock during the Class Period and suffered damages as a result  
17 of the securities law violations alleged herein.

#### 18 **B. Defendants**

19           20. Defendant Intel is a global technology company that designs and manufactures  
20 microprocessors and other semiconductor components that are used in computers, data centers,  
21 communications infrastructure, and other digital devices. The Company is incorporated in Delaware and  
22 maintains its corporate headquarters at 2200 Mission College Boulevard, Santa Clara, California. The  
23 Company’s Internet website address is [www.intel.com](http://www.intel.com). Intel stock trades on NASDAQ under the symbol  
24 “INTC.” As of January 15, 2021, Intel had over four billion shares of common stock outstanding, owned  
25 by thousands of investors. Throughout the Class Period, Intel disseminated SEC filings, press releases,  
26 investor presentations, and other materials containing material misrepresentations and omissions about  
27 the progress of its 7 nm chipmaking process and related topics.

1           21. Defendant Swan has served as Intel’s CEO and member of its Board of Directors since  
2 January 30, 2019. Immediately prior, Swan served both as the Company’s interim CEO (starting on  
3 June 21, 2018, upon the resignation of Intel’s former CEO, Brian M. Krzanich (“Krzanich”)) and its  
4 CFO, starting on October 10, 2016. On January 13, 2021, Intel issued a press release announcing that  
5 Swan would step down as Intel’s CEO as of February 15, 2021. Swan made or had authority over the  
6 content and dissemination of the false statements and omissions identified in Part VI below at ¶¶ 132-88,  
7 and is liable for those false statements and omissions. Swan also was a control person of Intel within the  
8 meaning of § 20(a) of the Exchange Act.

9           22. Defendant Davis has served as Intel’s CFO since April 3, 2019, when he joined the  
10 Company. Previously, Davis had served as the CFO of Qualcomm Inc. (“Qualcomm”) since March  
11 2013. Davis made or had authority over the content and dissemination of the false statements and  
12 omissions identified in Part VI below at ¶¶ 132-88, and is liable for those false statements and omissions.  
13 Davis also was a control person of Intel within the meaning of § 20(a) of the Exchange Act.

14           23. Defendant Renduchintala served as Intel’s Chief Engineering Officer and President of the  
15 Company’s Technology, Systems Architecture and Client Group (“TSCG”) from April 12, 2017, until  
16 his resignation on August 3, 2020. In these roles Renduchintala was responsible for, among other things,  
17 aligning technology, engineering, product design, and process development across all of Intel’s  
18 businesses. Before joining Intel in 2015, Renduchintala was an executive vice president at Qualcomm,  
19 and worked in the computing and mobile segments of its business. Renduchintala made or had authority  
20 over the content and dissemination of the false statements and omissions identified in Part VI below at  
21 ¶¶ 132-88, and is liable for those false statements and omissions. Renduchintala also was a control person  
22 of Intel within the meaning of § 20(a) of the Exchange Act.

23           24. Defendants Swan, Renduchintala, and Davis are collectively referred to herein as the  
24 “Individual Defendants,” and, together with Intel, are the “Defendants.”

25           25. Each of the Individual Defendants, by virtue of his high-level position with Intel, directly  
26 participated in the management of the Company, was directly involved in the day-to-day operations of  
27 the Company at the highest levels, and was privy to confidential and proprietary information concerning  
28 the Company and its business and operations. Because of their positions with Intel, the Individual

Defendants possessed the power and authority to control the contents of the Company's reports to the SEC, press releases, and presentations to investors and financial analysts. Each was involved in drafting, producing, reviewing, and/or disseminating the statements at issue in this case, approved or ratified these statements, or was aware or recklessly disregarded that these statements were being issued regarding the Company. As set forth below, the materially misstated information that Intel conveyed to the public was the result of the collective actions of these individuals. Because of their positions and access to material non-public information available to them, each of the Individual Defendants knew that the adverse facts specified herein had not been disclosed to, and were being concealed from, the public, and that the positive representations which were being made were then materially false and/or misleading.

#### **IV. OVERVIEW OF THE FRAUD**

##### **A. Background on Intel's Business**

##### **1. Intel's Products and Operating Groups**

26. Intel designs and manufactures microprocessors for use in computers, data center servers, communications devices and infrastructure, and other digital electronic devices. The Company divides its product portfolio into two divisions: (i) its "data-centric" lines of business, and (ii) its PC-centric line of business.<sup>1</sup> Intel's data-centric businesses include its Data Center Group ("DCG") and Programmable Solutions Group ("PSG"), among others. Intel's PC-centric business consists solely of its Client Computing Group ("CCG"), which encompasses the microprocessor chips used in laptop and desktop personal computers.

27. Historically, the CCG business generated the majority of Intel's total revenues.<sup>2</sup> More recently, however, Intel's data-centric business has contributed an increasing share of the Company's revenues, driven primarily by growing sales of the high-margin server CPU chips sold by the DCG group.<sup>3</sup> At year-end 2019, the vast majority of the Company's revenues was generated by Intel's CCG

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<sup>1</sup> See, e.g., Intel, Annual Report (Form 10-K), at 16 (Jan. 24, 2020).

<sup>2</sup> See, e.g., Intel, 2019 Investor Meeting CEO Presentation at 9 (May 8, 2019) (showing "PC-Centric Business" contributing approximately 70% of Intel's revenues in 2013.)

<sup>3</sup> See, e.g., Intel, 2019 Investor Meeting CEO Presentation at 9 (May 8, 2019) (showing "Data-Centric Business" contributing approximately 50% of Intel's revenues in 2018, with projected growth to over 70%).

1 and DCG businesses, which contributed 52% and 33%, respectively, to the Company's \$72 billion in  
2 2019 total revenues.<sup>4</sup> Intel's financial health, profitability, and future prospects are therefore inextricably  
3 linked with the status of its microprocessor design and manufacturing operations, which creates the  
4 products sold by the Company's CCG and DCG groups.<sup>5</sup>

5 28. On the manufacturing side, Intel's chip manufacturing organization was long known as  
6 the Technology and Manufacturing Group ("TMG"). TMG was historically the "superstar" within Intel;  
7 as set forth more fully below, its relentless pace of execution enabled Intel's success in the marketplace.  
8 In early 2018, Intel reorganized TMG, whose leaders had previously reported directly to Intel's CEO,  
9 under the new TSCG, which now reported directly to Renduchintala.

## 10 **2. Intel's Integrated Device Manufacturer ("IDM") Business Model**

11 29. Throughout its history, Intel has utilized an IDM business model for its most important  
12 products. This business model has been key to Intel's profitability, the value of its stock, and its  
13 attractiveness to investors. Under this vertically integrated model, Intel both designs *and* manufactures  
14 its "leading-edge" microprocessors at its in-house semiconductor fabrication (chipmaking) facilities,  
15 called "fabs." "Leading-edge" chips are the most advanced and cutting edge in terms of miniaturization,  
16 performance, and features, and represent the state-of-the-art in design and manufacturing technology.  
17 7 nm was Intel's "leading-edge" manufacturing process under development during the Class Period.

18 30. Key benefits of the IDM model include: (i) owning every important part of the design  
19 and manufacturing process, thus rendering production more efficient and cost-effective by eliminating  
20 any intermediaries; (ii) guaranteeing that the necessary manufacturing capacity is available at the right  
21 time to meet upcoming projected demand; and (iii) avoiding the risk of intellectual property loss due to  
22 the need to share details of chip design and manufacture with third-parties.

---

25 <sup>4</sup> See, e.g., Intel, Annual Report (Form 10-K), at 4, 16 (Jan. 24, 2020).

26 <sup>5</sup> Intel's notable CCG customers include laptop and desktop makers such as Dell, Lenovo, Hewlett  
27 Packard, Quanta, and SuperMicro. Intel's notable DCG customers, which purchase Intel's server  
28 products, include Google, Facebook, and Amazon (the so-called "hyperscalers,") which run massive data  
centers powered by a multitude of server racks, as well as other companies that make servers for a wide  
range of other customers.

1           31. Pursuant to this model, *only* Intel’s fabs have produced its most critical, advanced  
2 products, including its leading-edge central processing unit (“CPU”) processors used in desktops, laptops,  
3 and servers, and more recently other types of advanced chips. In contrast, when it made economic sense,  
4 Intel has outsourced to the foundries some production of its non-CPU components (such as chipsets) that  
5 are suitable for fabrication on older, trailing edge process nodes due to their more commoditized nature.  
6 Intel has also fabricated non-Intel designed chips elsewhere if they were already intended to be made at  
7 a competitor’s fab, such as chips acquired through acquisitions of other companies. In other words, Intel  
8 was an IDM for its most advanced chips, and semi-fabless for certain categories of other chips. Long  
9 before and during the Class Period, Defendants touted the Company’s IDM business model as a critical  
10 advantage over Intel’s competitors, even describing it as “foundational to our current and future success.”

11           32. In contrast to Intel’s IDM business model, Intel’s competitors (such as Advanced Micro  
12 Devices, Inc. (“AMD”), Nvidia Corp. (“Nvidia”), and Qualcomm) utilize a so-called “fabless” business  
13 model. Fabless chip companies primarily focus on chip design and marketing while contracting with  
14 outside foundries such as Taiwan Semiconductor Manufacturing Company, Ltd (“TSMC”) for chip  
15 manufacturing. Conversely, TSMC, a semiconductor manufacturer, leaves chip design to its customers.  
16 With its IDM business model, therefore, Intel competes both with foundries like TSMC and Samsung  
17 Foundry (“Samsung”) and with fabless chip designers like AMD, Nvidia, and Qualcomm.

18           33. For Intel’s IDM business model to prosper, Intel must maintain leadership in *both* the chip  
19 design *and* manufacturing spheres to harness the IDM model’s cost advantage and associated benefits to  
20 achieve favorable profitability. For more than two decades, Intel thrived under its IDM model.

### 21                   **3. The Microprocessor Design and Manufacturing Process**

22           34. Although techniques to make microprocessor chips have evolved, the process has largely  
23 remained the same – both for Intel and its competitors. The chip (or “die”) is designed using software to  
24 lay out the circuit patterns necessary to accomplish each of its intended functions. Once the design work  
25 is completed, the chip is ready for “tapeout,” which marks the completion of the initial processor design  
26 and verification steps. The chip specifications are then sent to the fab to begin the physical manufacturing  
27 process.

1           35. At the fab, silicon wafers progress through a months-long, largely automated  
2 manufacturing journey. During this process, the chip’s structures are etched onto the wafer surface, layer  
3 by layer, using a process known as photolithography.<sup>6</sup> These structures are then connected by metal  
4 wiring into circuits. At first, only test wafers are run through the fab to ensure that the chips can be  
5 manufactured according to specifications and with adequate yield (as discussed below). Only then can  
6 the fab “ramp” production by manufacturing regular wafers in higher volumes.

#### 7                   **4. Microprocessor Manufacturing Yields**

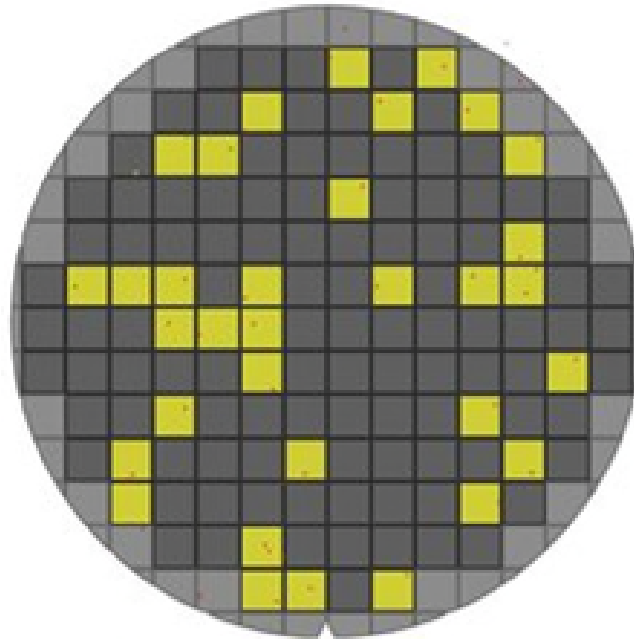
8           36. One silicon wafer can contain dozens, hundreds, or even thousands of individual  
9 microprocessor die, depending on their size and intended purpose. However, it is common for some  
10 percentage of the die on each wafer to be only partially functional or non-functional due to various defects  
11 that can occur throughout the manufacturing process. The measure of “good” and “bad” die on each  
12 wafer is known as its “yield,” which is among the most important metrics in semiconductor  
13 manufacturing.

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26  
27  
28 <sup>6</sup> In the last several years, leading-edge foundries such as TSMC have utilized Extreme Ultraviolet  
Lithography (“EUV”) to manufacture their newest and most advanced 7 nm and 5 nm chips. However,  
as discussed below (and contrary to Defendants’ representations to investors), Intel has thus far proven  
unable to effectively utilize EUV to manufacture its own 7 nm chips.



37. A fabrication process's yield serves as a critical proxy for its health – the more die that come off each wafer working as intended, the higher the yield, and thus the healthier that process is. Yield is measured on a percentage basis. For example, on a wafer designed to have 132 total working die, if 33 die were defective, and 99 die were functional, this wafer would have a yield of 75% (or 99 functional die divided by 132 total die), as depicted below.



*Figure 1: A silicon wafer with 132 total individual die. If 33 are defective (yellow) and 99 are functional (dark grey), the yield of this wafer is 75%.*

38. Every effort is made to improve yields as quickly as possible in order to commence high-volume manufacturing. Intel has historically sought to ramp yields to reach “healthy” yield levels (generally considered to start above 50%, depending on numerous factors) on a new manufacturing process node as quickly as possible before ramping into high-volume manufacturing. A failure to improve yields to viable levels in a timely manner can lead to severe negative economic, competitive, and reputational consequences for a chip maker.

## 5. Moore's Law and the Economics of Microprocessor Innovation

39. In the mid-1960s, Intel co-founder Gordon Moore ("Moore") observed that every two years, the number of transistors that could be fabricated within a given area on the surface of a microprocessor had been doubling. This doubling of transistor density came to be widely known as "Moore's Law." Moore forecast that this trend would continue.<sup>7</sup> The computer hardware and software industries adopted the economic implications of Moore's Law as a goal to guide their development efforts. In conformance with Moore's Law, the price, performance, and power efficiency of microprocessor chips have improved dramatically over the last half-century. Below is an illustration of Moore's Law in action:

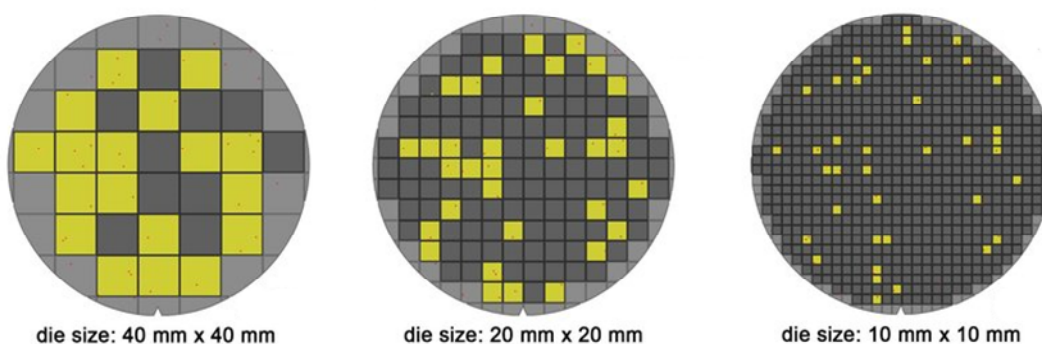


Figure 2: Moore's Law in action: doubling the number of transistors that can be fit on the same unit area means a same-sized silicon wafer can fit many more chips.

40. Critically, whichever company first moved to a new and smaller process node enjoyed a significant comparative economic advantage over its competitors. If a company's chip product was even slightly better than a competitor's in some key metric (such as price, performance, or power consumption), it often captured an outsized portion, or even the vast majority, of revenue for that market segment. More often than not, Intel was the industry leader in this high-stakes "winner-take-all" scenario and profited handsomely as a result. This was possible because Intel's process leadership and in-house manufacturing capability (through its IDM model) allowed it to produce its chips at costs far lower than its competition. It could thus put pressure on its competitors' chip pricing, while maintaining superior performance for its customers and enviable profit margins for itself.

<sup>7</sup> See, e.g., Mark Bohr, *Intel Co-Founder Gordon Moore Receives IEEE Medal Of Honor* (Sept. 20, 2008), [https://blogs.intel.com/technology/2008/09/intel\\_co-founder\\_gordon\\_moore/](https://blogs.intel.com/technology/2008/09/intel_co-founder_gordon_moore/).

1           **B.     Intel Badly Falters in Developing Its 10 nm Chip, Allowing Its**  
2           **Competitors to Overtake Intel's Technology and Gain Market Share**

3           41.     Between approximately 2000 and 2011, Intel had progressed from a 130 nm process node  
4 down to 22 nm, in lockstep with the timeframes set forth by Moore's Law.<sup>8</sup> Intel dubbed this regular  
5 cadence of improvements its "Tick-Tock" production model. Under this model, each "tick" represented  
6 a shrinking of the process node technology to a new, smaller size, while each "tock" designated the  
7 implementation of a new chip microarchitecture (i.e., improvements on the chip's design, added features,  
8 or both).<sup>9</sup> AMD and other companies that had sought to challenge Intel's industry leadership found it  
9 difficult to surmount Intel's relentless "Tick-Tock" cadence and lagged behind Intel in the technology  
10 "arms race." With the release of its 22 nm chips in 2011, Intel was a full process node ahead of the rest  
11 of the leading-edge foundries. Intel's next planned "tick," was to be a shrink of the existing 22 nm  
12 architecture to be fabricated on a smaller 14 nm process node.

13           42.     In contrast to the transitions that had marked Intel's previous node shrinks for more than  
14 a decade, however, Intel's transition to 14 nm was marred by setbacks and numerous delays. While  
15 initial 14 nm production was planned to commence in late 2013, these delays ultimately meant it did not  
16 reach the market in large quantities until the first half of 2015, more than a year late.<sup>10</sup>

17           43.     Difficulties and delays were not isolated to the 14 nm process, however. By late 2015,  
18 Intel had not "ticked" to its next, smaller process node, 10 nm. Instead, Intel announced that it was  
19 pushing back the launch of its first 10 nm chips until the second half of 2017.<sup>11</sup> However, in 2017, Intel  
20 was still facing unacceptably low yields on its 10 nm process. Well into 2018, Intel encountered low

21           <sup>8</sup>     See Kelin Kuhn, *IDF, skeptical students, 22nm and the relentless pursuit of Moore's Law*  
22 (Apr. 15, 2010), [https://blogs.intel.com/technology/2010/04/idf\\_interviewing\\_students\\_22nm/](https://blogs.intel.com/technology/2010/04/idf_interviewing_students_22nm/).

23           <sup>9</sup>     See Intel, *The Tick-Tock Model Through the Years*,  
24 <https://web.archive.org/web/20191104235556/https://www.intel.com/content/www/us/en/silicon-innovations/intel-tick-tock-model-general.html>.

25           <sup>10</sup>    See, e.g., Brooke Crothers, *Intel CEO talks delayed factory, 'Broadwell' production start*, C|Net  
26 (Jan. 16, 2014), <https://www.cnet.com/news/intel-ceo-talks-delayed-factory-broadwell-production-start/>; Thomas Ryan, *Intel Admits to Broadwell Delays in its Q2 Call*, SemiAccurate (July 18, 2014),  
<https://www.semiaccurate.com/2014/07/18/intel-admits-broadwell-delays-q2-call/>.

27           <sup>11</sup>    See, e.g., Brett Howse & Ryan Smith, *Tick Tock On The Rocks: Intel Delays 10nm, Adds 3<sup>rd</sup> Gen*  
28 *14nm Core Product "Kaby Lake,"* AnandTech (July 16, 2015),  
<https://www.anandtech.com/show/9447/intel-10nm-and-kaby-lake>.

1 yields on its 10 nm process and had yet to ramp into high-volume production.<sup>12</sup> At Intel’s May 17, 2018  
2 Annual Shareholder meeting, Krzanich announced that “the yields on this product haven’t come up as  
3 quickly as we wanted [them] to,” and that Intel was therefore “going to slow the ramp down of 10  
4 nanometers” until yields could be improved “as we move into 2019.”

5 44. On June 21, 2018, Intel announced Krzanich’s immediate resignation due to discovery of  
6 a “past consensual relationship with an Intel employee.”<sup>13</sup> Numerous industry observers, however, cast  
7 doubt on the public explanation for Krzanich’s ouster and questioned whether the actual reason was the  
8 years-long floundering of Intel’s 10 nm process node.<sup>14</sup> The same day, Defendant Swan (Intel’s then-  
9 CFO) was announced as the Company’s interim CEO.

10 45. On July 26, 2018, during Intel’s Q2 2018 earnings call, Swan stated that Intel did not  
11 “expect [10 nm] systems on shelves [before] the 2019 holiday season.” In the meantime, Intel had been  
12 continuing to release a series of incremental 14 nm chip “optimizations” – rehashes of the same  
13 fundamental process and architecture that Intel had been using since 2013.

14 46. While Intel was suffering continual 10 nm delays, its foundry competitors, principally  
15 TSMC and Samsung, were moving to parity with the Company in terms of their own process technology  
16 advances. For example, in 2015, Samsung began mass production of its own 14 nm chips, with 10 nm  
17  
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20

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21 <sup>12</sup> See, e.g., Charlie Demerjian, *Intel guts 10nm to get it out the door*, SemiAccurate.com (Aug. 2,  
22 2018) (reporting that as of mid-2018 “things have improved” since the initial 8-10% yields on Intel’s  
23 10 nm Cannon Lake, “but not much, think increments not multiples,” and that “progress is at a standstill”  
in terms of actually fixing the yield problems), <https://www.semiaccurate.com/2018/08/02/intel-guts-10nm-to-get-it-out-the-door/>.

24 <sup>13</sup> See Intel, *Intel CEO Brian Krzanich Resigns; Board Appoints Bob Swan as Interim CEO*  
25 (June 21, 2018), <https://newsroom.intel.com/news-releases/intel-ceo-brian-krzanich-resigns-board-appoints-bob-swan-interim-ceo/>.

26 <sup>14</sup> See, e.g., Charlie Demerjian, *Brian Krzanich out as CEO of Intel*, SemiAccurate.com (June 21,  
27 2018), <https://www.semiaccurate.com/2018/06/21/brian-krzanich-out-as-ceo-of-intel/>; Charlie  
28 Demerjian, *Intel’s firing of CEO Brian Krzanich is a cover for deeper problems*, SemiAccurate.com  
(June 29, 2018), <https://www.semiaccurate.com/2018/06/29/intels-firing-of-ceo-brian-krzanich-is-a-cover-for-deeper-problems/>.

chips following in 2017.<sup>15</sup> Similarly, in 2014, TSMC introduced a 20 nm process, followed by a 16 nm process in 2015, a 10 nm process in 2016, a 7 nm process in 2018, and a 5 nm process in 2019.<sup>16</sup>

47. By late 2018, TSMC's 7 nm process began its ramp to high-volume chip production,<sup>17</sup> while Intel's own comparable 10 nm process continued to remain stymied by yield problems preventing any widescale product launch.<sup>18</sup>

48. With Intel floundering, competitors AMD and TSMC formed a strategic alliance and began making chips containing revolutionary design changes at smaller process nodes that allowed them to begin capturing market share from Intel.

49. AMD and TSMC's fabless-foundry alliance meant that as TSMC's accelerating technological advancements allowed it to close its manufacturing process gap with Intel's fabs, AMD's competitive positioning with respect to Intel was commensurately strengthened. For example, AMD's "Zen 2" data center and consumer processors were designed around TSMC's 7 nm process and were highly competitive with Intel's aging 14 nm offerings on both price and performance. Moreover, AMD's "Zen 3" and subsequent chip roadmap centered on TSMC's 5 nm and future process nodes.

50. This emerging competition put further pressure on Intel to catch up by finally moving past 14 nm to 10 nm and 7 nm. Intel thus faced the prospect of serious and escalating competition from AMD

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<sup>15</sup> See, e.g., Samsung, History: Present-2005, <https://www.samsung.com/us/aboutsamsung/company/history/>.

<sup>16</sup> See, e.g., TSMC, Logic Technology, <https://www.tsmc.com/english/dedicatedFoundry/technology/logic.htm>.

<sup>17</sup> See, e.g., Rick Merritt, *TSMC's Roadmap Full, But Thin*, EETimes (May 2, 2018) (reporting that TSMC "is in volume production with a 7-nm process and will have a version using extreme ultraviolet (EUV) lithography ramping early next year" and "aims to start risk production of a 5-nm node in the first half of 2019, focusing on mobile and high-performance computing chips.").

<sup>18</sup> See, e.g., Charlie Demerjian, *Intel's firing of CEO Brian Krzanich is a cover for deeper problems*, SemiAccurate.com (June 29, 2018) ("Intel has known how bad things are [on 10 nm] for quite literally years and hasn't been telling the truth. . . . A good example of this is the claim that 10nm is shipped in 2017. Technically Intel is correct, it did ship in the last remaining seconds of 2017 in volumes you could keep in one of your pants pockets. And we can go on but we already covered this in detail back in May. Yields of fully working chips rounds to zero. Intel's 10nm process flat out doesn't work . . . . If you understand semiconductor fabrication, you know it doesn't take 18-21 months to implement a known fix. . . . According to the company it is already shipping, already doing well, and volume is just around the corner, see why we say zero credibility?"), <https://www.semiaccurate.com/2018/06/29/intels-firing-of-ceo-brian-krzanich-is-a-cover-for-deeper-problems/>.

for the first time in years (as well as from every other competitor utilizing TSMC’s production capabilities for other types of chips, such as Nvidia’s GPUs, Qualcomm’s communications chips, and later, Apple’s ARM laptop CPUs).

51. As shown below, by partnering in 2017 with TSMC on increasingly sophisticated 7 nm chips—while Intel continued its iterations of 14 nm designs—AMD’s market share began to grow steadily, all at Intel’s expense.

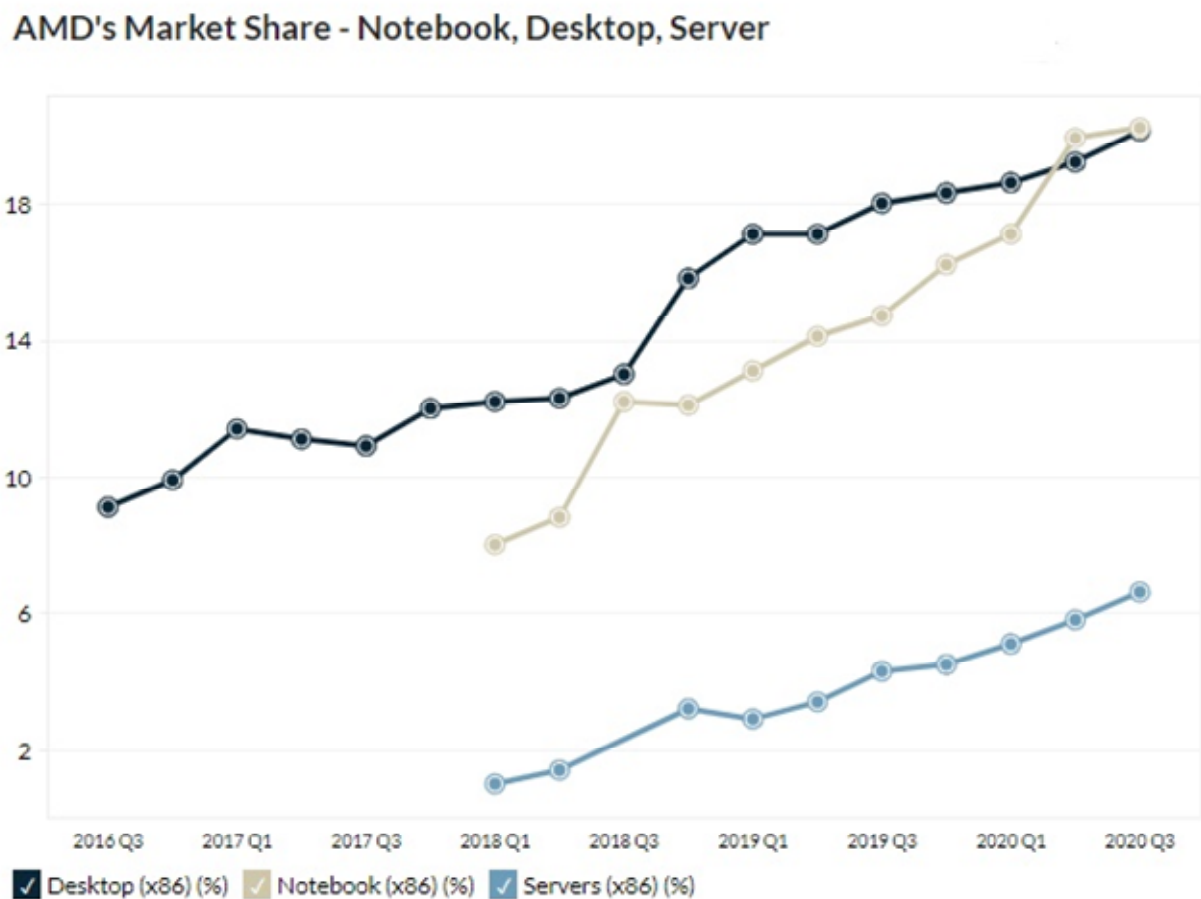


Figure 3: “AMD’s Market Share – Notebook, Desktop, Server”

52. These developments underscored the importance to Intel of convincing its customers and investors that it would be ready to move promptly to the next generation process node: 7 nm.



1           **C.     Leading Up to the Class Period, Defendants Repeatedly Assure the Market**  
2           **that They Are Intensely Focused on Developing the 7 nm Process on Time,**  
3           **and Would Not Repeat the Errors and Delays of the 10 nm Process**

4           53.     For the reasons noted above, Intel's progress on 7 nm was a topic of intense focus for  
5 investors and analysts during earnings calls leading up to the Class Period. Intel's ability to convince the  
6 market of its progress towards 7 nm chip production was of paramount importance to the Company.

7           54.     Beginning in at least April 2018, Intel began reassuring analysts and investors that its  
8 next-generation 7 nm process would not suffer the same problems and setbacks as 10 nm. For example,  
9 on April 26, 2018, during Intel's Q1 2018 earnings call, then-CEO Krzanich stated that Intel had  
10 employed an "overly aggressive" scaling factor of 2.7 in its shrink of the 14 nm process down to 10 nm,  
11 which was considerably greater than its previous scaling factors of 2.4 or less. Krzanich explained that,  
12 consequently, "we made a lot of changes at 7 nanometers. . . . We're going back to a more standard for  
13 us compaction number of 2.4[.] So that makes it a little bit easy. . . . So really, 7 nanometers is quite a  
14 bit different, and so I think as a result, we don't expect to see these kinds of impacts on 7 nanometers."

15           55.     That same day, media reports surfaced regarding industry veteran and renowned  
16 microprocessor architect Jim Keller ("Keller") joining Intel.<sup>19</sup> Keller had gained a reputation of "creating  
17 chip designs 'that turn companies around,'" <sup>20</sup> leading industry observers to believe that Intel's purpose  
18 in hiring him, among other things, was to help stabilize its struggling 10 nm program as well as set it on  
19 a course to combat emerging competitive threats and reinvigorate Intel's pipeline of innovation.

20           56.     At the Company's May 17, 2018 Annual Shareholder meeting, an analyst asked whether  
21 "the challenges you had on 10 nanometers [will] impact 7-nanometer execution," and Krzanich answered  
22 that "most of the problems that we encountered on 10-nanometer will not impact 7-nanometer." Krzanich  
23 affirmed that "we continue to monitor our progress on 7 nanometers and continue to be very positive  
24 about where we're at with 7 nanometers."

25  
26 <sup>19</sup>     See Ted Greenwald, *Intel's Higher Profit Shows Firm Shaking Off Chip Flaws*, Wall St. J. (Apr. 26, 2018), <https://www.wsj.com/articles/intels-profit-revenue-increase-1524774068>.

27 <sup>20</sup>     See Tim Higgins and Ted Greenwald, *Tesla's Autopilot Hit With More Turmoil as Leader Departs*  
28 *for Intel*, Wall St. J. (Apr. 26, 2018), <https://www.wsj.com/articles/teslas-autopilot-hit-with-more-turmoil-as-leader-departs-for-intel-1524723484>.

1           57.     On July 26, 2018, during Intel’s Q2 2018 earnings call, Renduchintala was asked about  
2 the timing of 7 nm, and “what you’ve learned on 10, how you’re applying it to 7 and . . . how it’s going.”  
3 Renduchintala explained that “7 [nm] is very much R&D in deep progress and we’re making good  
4 progress on that development,” and that “key learnings” from Intel’s 10 nm experience were being  
5 applied to its 7 nm development. Renduchintala added that Intel was “focusing on being much more  
6 precise in our ability to launch,” and that “we monitor progress on 7 just as closely as we are on 10, I feel  
7 those lessons are being well absorbed into our progress.”

8           58.     During Intel’s April 25, 2019 Q1 earnings call, Swan stated that Intel was “currently  
9 architecting what we expect will be the United States’ first exascale supercomputer for the [DOE]’s  
10 Argonne National Laboratory . . . called Aurora, [which] will be delivered in 2021 and powered by Intel  
11 technologies . . . .” Specifically, Aurora would include “a future generation of the Intel Xeon Scalable  
12 [server] processor,” among other components. As noted below, Project Aurora was later revealed to be  
13 powered by Intel’s first chip built on its advanced 7 nm process.<sup>21</sup>

14           59.     Aurora represented a prestigious feather in Intel’s cap that would produce a halo effect  
15 over its leading-edge processes and products and serve as an important strategic geopolitical milestone  
16 as the lead U.S. effort in the international exascale “arms race.” Aurora also represented a record  
17 government contract for Intel, as well as an opportunity for Intel to vindicate its earlier stumbles with the  
18 prior 10 nm iteration of Aurora. Aurora also would allow Intel to showcase its competitive progress with  
19 respect to key rivals AMD and TSMC, as DOE planned to follow Aurora’s deployment with two  
20 additional exascale systems, called Frontier and El Capitan (for its Oak Ridge and Lawrence Livermore  
21 National Laboratories, respectively), both of which would be powered by rival AMD’s components  
22 (fabricated by TSMC).

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23  
24  
25 <sup>21</sup> Aurora followed on the heels of an earlier DOE effort (also called Aurora) to create a less  
26 sophisticated “petascale” capable supercomputer, which was abandoned by DOE when Intel failed to  
27 supply a 10 nm chip critical to the effort. *See, e.g.,* Joel Hruska, *Intel Quietly Kills Off Xeon Phi*,  
28 *ExtremeTech.com* (May 8, 2019) (noting Intel’s “Knights Hill” chip “was killed off several years ago,  
[and] was originally intended for 10nm and 2016” and that “Intel killed Knights Hill in November 2017”  
which “pushed back the introduction of the Aurora supercomputer”) <https://www.extremetech.com/extreme/290963-intel-quietly-kills-off-xeon-phi>.



60. On May 8, 2019, Intel held its “2019 Investor Meeting,” during which Swan officially announced that “our intention is to accelerate 7-nanometer. We’ve obviously been working on this for a while and we expect production and launch of 7-nanometer products in 2021.” As part of his presentation, Swan displayed this slide:



Figure 4: Slide from Swan’s 2019 Investor Meeting presentation stating that Intel would “ACCELERATE TO 7NM” with “Production and Launch in 2021 vs. TSMC 5 NM.”

61. Renduchintala further expanded upon Swan’s announcement, stating that “7-nanometers will be the fullest realization of our new approach, incorporate all the lessons that . . . we’ve learned in 14 and 10. We’ve made schedule and time-to-market a priority.” Later in the meeting, Renduchintala reiterated that “[w]e’ve learned from our 10-nanometer experiences . . . and we’ve institutionalized and driven those [lessons] into our definition of 7-nanometers, and we’re executing at full pace per the original schedule that we set out 2 years ago on that 7-nanometer road map.”

62. Renduchintala also provided additional information regarding the Aurora supercomputer that Swan had referenced during the Q1 2019 earnings call, stating “as Bob [Swan] also let out of the bag, we plan to launch our [7 nm] lead product in 2021. . . . I’m excited to unveil our first and lead 7-nanometer product [Ponte Vecchio]. It’ll be a groundbreaking GP-GPU product targeted for our data center and HPC [high performance computing] applications, a major strategic priority for Intel. . . . The

product will launch in 2021 and its the basis of the previously announced design win with the [DOE] to deliver the U.S.'s first exaflop computer, Aurora.” During his presentation, Renduchintala displayed the following slide stating that “7nm progressing to plan” and “Lead product launch in 2021.”<sup>22</sup>

63. Later in his comments, Renduchintala also noted that after Ponte Vecchio, “[t]he next product on 7-nanometer will be a data center CPU. . . . [A] data center GPGPU followed by a data center CPU is the way we’re planning a road map.” Renduchintala also reminded the audience to “[r]emember, we’ve really simplified the design axiom for 7-nanometer. So you’re going to see a much, much faster flow-through of products through our nodes than you traditionally measured us by. The idea is simple processes, balanced scaling, large product volume through the node at a much earlier time period.”

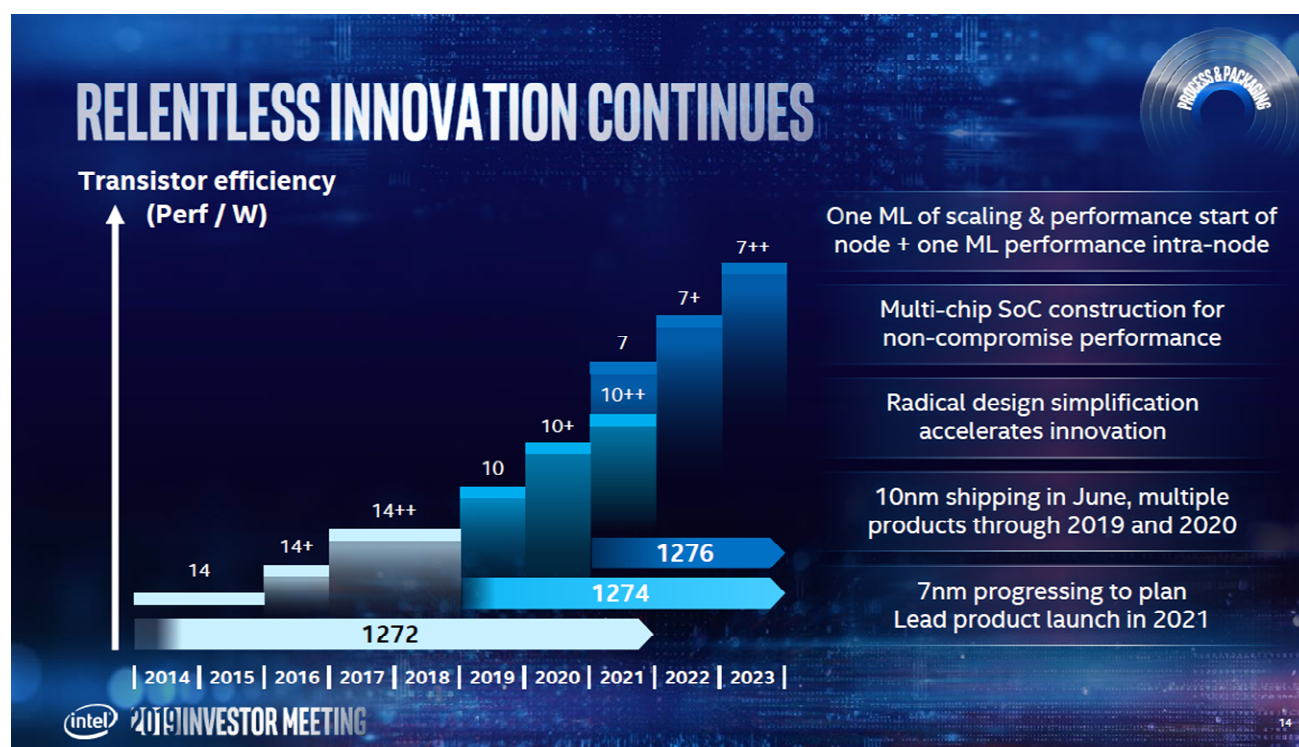


Figure 5: Slide from Renduchintala’s 2019 Investor Meeting presentation, depicting Intel’s process node timeline and stating that “7nm progressing to plan” and “Lead product launch in 2021.”

<sup>22</sup> On May 8, 2019, Intel published this same slide on its online “newsroom.” See “2019 Investor Meeting: Intel Previews Design Innovation; 10nm CPU Ships in June; 7nm Product in 2021” (May 8, 2019), <https://newsroom.intel.com/news/2019-intel-investor-meeting/#gs.pzwvw7> (“[T]he 7nm general purpose GPU is expected to launch in 2021.”). The next day, Intel filed its 2019 Investor Meeting slides with the SEC. See Intel, Current Report (Form 8-K) at Ex. 99-2, at 14 (May 9, 2019).

64. Also during the 2019 Investor Meeting, Navin Shenoy, Executive VP & GM of DCG (“Shenoy”), told investors that Intel planned to “accelerate the pace” of its Xeon server CPU roadmap such that Intel would introduce its 10 nm server CPU, “Sapphire Rapids,” by “2021,” and its “next gen [server CPU] after that” in “2022”—i.e., the “7-nanometer . . . data center CPU” that Renduchintala had just told investors would be Intel’s “next product” after Ponte Vecchio. Shenoy displayed the following slide depicting “Sapphire Rapids” in “2021” and “Next Gen” in “2022”:

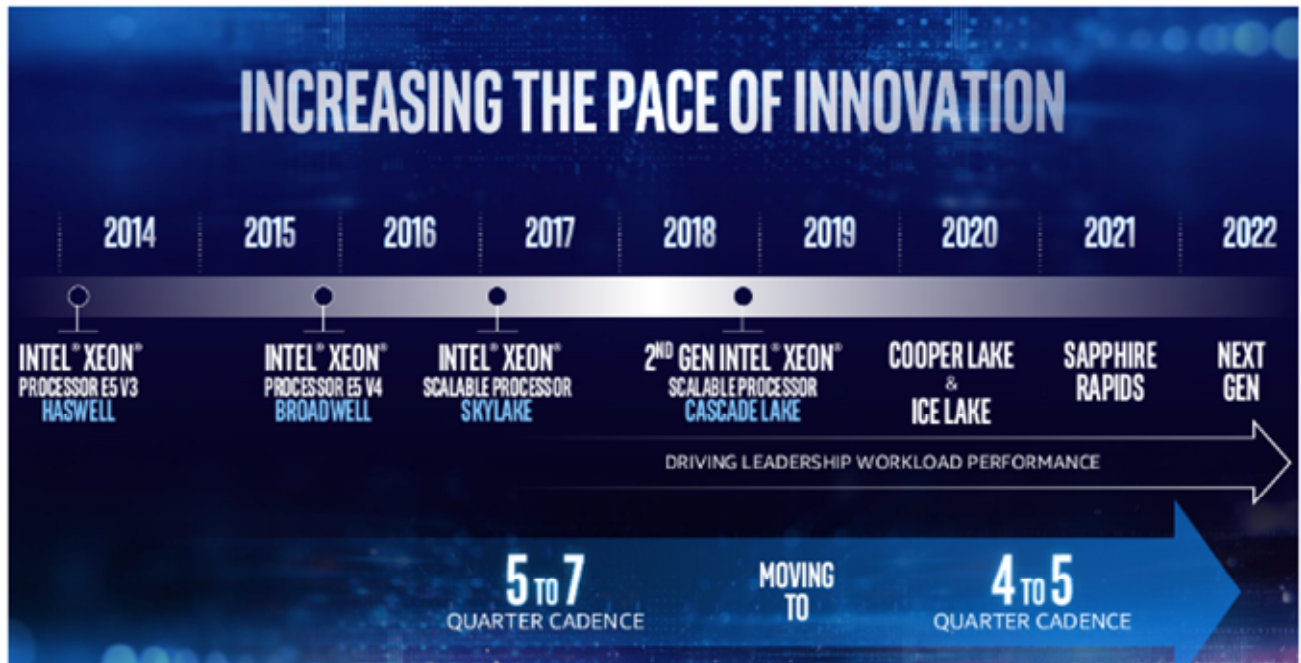


Figure 6: Slide from Shenoy’s 2019 Investor Meeting presentation depicting Intel’s “INCREASING PACE OF INNOVATION” with the launch of “SAPPHIRE RAPIDS” in “2021” and “NEXT GEN” in “2022.”

65. On July 25, 2019, during Intel’s Q2 earnings call, Swan again stated that Intel was “on track to launch 7-nanometer in 2021,” and noted that “[w]ith a roughly 2x improvement in density over 10-nanometer, our 7-nanometer process, which will be comparable to competitors’ 5-nanometer nodes, will put us on pace with the historical Moore’s Law scaling.”

**D. Throughout the Class Period, Defendants Falsely Assure Investors that Intel’s Initial 7 nm Technology Was “on Track” for Its 2021 Launch, with the 7 nm Data Center CPU Product Following in 2022**

66. As noted above, the market was keenly focused on the timing and health of Intel’s 7 nm process node. The development and launch of 7 nm, if delivered on time and with acceptable yields, would serve as a meaningful boost to Intel’s efforts to reestablish its process node leadership in the industry and put behind it the years-long debacle that the 10 nm node problems posed to the Company.

67. Conversely, any hint of trouble with Intel's 7 nm progress could signal to the market a return to the years of delays, disappointments, and erroneous messaging that defined Intel's 10 nm era.<sup>23</sup>

68. Thus, throughout the Class Period, Defendants repeatedly reassured the market that Intel's 7 nm process was "on track" and "making good progress" such that (i) its flagship 7 nm Ponte Vecchio chip would launch in Q4 2021, and (ii) Intel would quickly follow-up Ponte Vecchio with a "full portfolio" of 7 nm CPUs, including 7 nm server CPUs for data centers, by 2022.

69. For example, on October 24, 2019, Swan assured the market that "[w]e are on track to launch our first 7-nanometer-based product, a data center-focused discrete GPU [Ponte Vecchio], in 2021, 2 years after the launch of 10-nanometer," and that "we'll get back on a 2-year cadence in 7 [nm] and beyond. So lots of learnings out of 10-nanometer that we've incorporated."

70. Both analysts and the market were swayed by Swan's positive 7 nm message. Intel's common stock opened the next day (October 25, 2019) at \$54.19 per share, up \$1.96 (3.75%) over the prior day's closing price, and went on to finish that day's trading at \$56.46, up \$4.23 (8.10%) over the prior day's closing price. In the wake of Swan's positive messaging regarding Intel's 7 nm outlook, Deutsche Bank rated Intel "Buy" with a \$62.00 price target, stating "[w]e applaud the company's aggressive tack towards fixing its manufacturing and accelerating its product roadmap," and praised Intel's "aggressive manufacturing roadmap (10nm on track in 2H19, 7nm in 4Q 2021) . . . ." Similarly, Credit Suisse analysts praised the "[g]oodness" of Intel's "return to a 2-2.5 year Moore's Law cadence," upgraded their price target for Intel's stock to \$65.00 per share, and rated the Company "Outperform."

71. On December 3, 2019, Swan told investors that "we didn't start it [7 nm] yesterday. We started several years ago and we monitor performance on density, on functionality and based on kind of where we are today, we feel pretty good about getting to a two, 2.5 year cadence and launching our first 7-nanometer product in the fourth quarter of 2021."

72. To bolster their claims that 7 nm was "on track" and "making good progress," the Individual Defendants also emphasized the "lessons learned" from Intel's 10 nm development and yield ramping process, and how those lessons had been applied to Intel's 7 nm design and development. For

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<sup>23</sup> See, e.g., *supra* note 18.



example, on December 10, 2019, Defendant Renduchintala described how the “four key lessons” learned “on 10” were “integrated into our approach on 7.” Specifically, these lessons included “balanc[ing] the pursuit of scaling and cost together with schedule predictability power and performance”; “continu[ing] to harvest intra-node product optimizations or intra-node process optimizations”; “maintain[ing] a mix of [process] nodes”; and “mak[ing] it easy and fast for our design teams to be able to migrate through intra-node transitions.” “[A]s a result of” these “lessons,” Renduchintala stated that “we’re making good progress on 7 . . . . And as we’ve announced previously, we’ll see our first 7 nanometer product shipping in 2021 with a full [7 nm] portfolio in 2022.”

73. Analysts welcomed Renduchintala’s positive narrative regarding 7 nm. For example, later that same day, UBS analysts reported that “[Intel] noted that it had learned the lessons from 10nm challenges”; “[Intel] is now taking a more pragmatic approach to 7nm”; “GPGPU as lead product for 7nm”; “[Intel] . . . sees the GPGPU as an ideal architecture to ramp up process yields”; and “[Intel] indicated that there would be no large gap between GPGPU (we think H2;21) and the rest of the 7nm portfolio w/- entire product portfolio on 7nm within a year of GPGPU launch[.]” UBS gave Intel’s stock a “12-month rating” of “Buy” and a “12m price target” of \$60.00.

74. However, as discussed below, Defendants’ statements that Intel was “on track” to launch its initial 7 nm product in 2021, with a full portfolio in 2022, were false and misleading.

**E. In Reality, Unbeknownst to Investors, Intel Was Not “on Track” to Launch Its 7 nm Chips in 2021 or the Full 7 nm Portfolio in 2022**

**1. By No Later than December 12, 2019, Intel’s Internal Product Roadmaps Already Showed that Its 7 nm Server CPUs Were at Least a Year Behind the Publicly-Announced Launch Date**

75. On December 12, 2019, technology news website SemiAccurate published a report stating that Intel’s internal product roadmaps showed that its 7 nm server CPUs were already at least a year behind the publicly announced launch date—facts that were directly at odds with Defendants’ reassurances to investors. SemiAccurate is an online publication whose editor, Charlie Demerjian, is a “veteran technology journalist.”<sup>24</sup> Numerous financial analysts and journalists covering the

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<sup>24</sup> See Ashley Vance, *Hewlett-Packard and Dell Avoid Big PC Party*, N.Y. Times (June 5, 2009), <https://bits.blogs.nytimes.com/2009/06/05/hewlett-packard-and-dell-avoid-big-pc-party/>.

1 semiconductor sector have cited SemiAccurate’s articles, including on the specific issue of delays at Intel.  
2 For example, on May 6, 2011, *Barron’s* published an article stating that, according to a report by  
3 Longbow Research analyst Joanne Feeney, Mr. Demerjian “is well-respected in tech circles and has been  
4 right in past observations . . . .”<sup>25</sup> On December 12, 2019, Wells Fargo Securities published an analyst  
5 report noting that “[s]ome of our recent industry checks, and now including an article published by  
6 *SemiAccurate* this morning . . . , have suggested that Intel’s 10nm *Ice Lake* Xeon Scalable Processor  
7 roadmap could be slipping further.” On December 19, 2019, Susquehanna “host[ed] a conversation with  
8 SemiAccurate’s Charlie Demerjian to discuss his expectations for the increasingly competitive  
9 computing space in 2020.” On July 14, 2020, Susquehanna also hosted a “call with SemiAccurate . . . to  
10 discuss Intel’s server roadmap timeline.” On July 16, 2020, Wells Fargo Securities published an analyst  
11 report citing “a recent *SemiAccurate* article on potential delay vs. anticipated 4Q20 launch” of Intel’s  
12 “10nm *Ice Lake*” product.<sup>26</sup> On November 13, 2020, Morgan Stanley published an analyst report  
13 crediting “Semiconductor blog ‘SemiAccurate’” for reporting “that Intel was delaying its server version  
14 of ‘Ice Lake’ again” and confirmed that “[w]e checked with Intel and it does appear that there have been  
15 some short term issues with a late stage validation that per the company should delay shipments by ‘a  
16 matter of a few weeks.’” And on December 15, 2020, Susquehanna hosted a “call with SemiAccurate  
17 Founder Charlie Demerjian . . . to discuss the latest in manufacturing happenings at Intel and others”  
18 including “the latest updates on Intel’s manufacturing timelines, outsourcing, AMD competition and  
19 more (Milan, Xilinx), NVDA, MRVL/INPH, and supply shortages.”

20 76. SemiAccurate has been frequently credited with publishing breaking news about the  
21 semiconductor industry. For example, in August 2010, SemiAccurate broke news of Sony admitting to  
22 defective graphics chips in some of its laptops.<sup>27</sup> Likewise, in June 2011, SemiAccurate published a story

23  
24 <sup>25</sup> See Tiernan Ray, *Intel Sags, ARM Jumps on Rumor Apple May Switch (Update)*, *Barron’s*  
(May 6, 2011), <https://www.barrons.com/articles/BL-TB-32609>.

25 <sup>26</sup> SemiAccurate’s articles have been cited by *The New York Times*, *The Guardian*, *Barron’s*, *The*  
26 *Seattle Times*, *San Jose Mercury News*, *Dow Jones Institutional News*, *Dow Jones News Service*, *The*  
27 *Times Union*, *The Oregonian*, *Portland Business Journal*, *Asbury Park Press*, *The Business Review*, and  
*Computing*.

28 <sup>27</sup> See Charlie Demerjian, *Sony admits to 14 defective Nvidia notebooks*, *SemiAccurate.com*  
(Aug. 10, 2009), <https://semiaccurate.com/2009/08/10/sony-admits-14-defective-nvidia-notebooks/>.

1 detailing the scandal that led AMD, Nvidia, and VIA to leave Intel as the lone semiconductor design  
2 company in the BAPCo consortium.<sup>28</sup> And in August 2011, SemiAccurate published two stories, one  
3 covering the specifications of Nvidia's unreleased mobile graphics line up,<sup>29</sup> and another covering the  
4 specifications of AMD's (one of Nvidia's direct competitors) unreleased mobile graphics line up.<sup>30</sup>

5 77. The majority of SemiAccurate's December 12, 2019 report on Intel's 7 nm delay was  
6 behind a paywall requiring a \$1,000 subscription. The publicly available portion of SemiAccurate's  
7 article stated, in part, that "[i]t looks like Intel is not just delaying a single server project, their entire  
8 roadmap has just slid significantly. SemiAccurate is now worried about what we are hearing from the  
9 company, things do not appear to be getting better." To paying subscribers, however, the SemiAccurate  
10 article further elaborated that "SemiAccurate's sources say that Granite [Rapids, Intel's 7 nm server  
11 CPU] has now been pushed back to 2H 2023" and that "Intel repeatedly claims we will see 7nm server  
12 CPUs in 2021 but their roadmaps unquestionably say that is late 2023." SemiAccurate concluded that  
13 "[e]ither Intel's top management is so untethered from what is happening at the engineering level or  
14 someone is bending the facts to a very scary degree" and "[t]hings have been slipping for so long now,  
15 interrupted by the occasional big slide, it looks cultural." The full article stated:

16 *Note: the following is analysis for professional level subscribers only.*

17 \* \* \*

18 **The first realistic chance for Intel to surpass AMD was Sapphire's successor called**  
19 **Granite Rapids. [Granite Rapids] was due to be released in 1H 2022 or about where**  
20 **Sapphire is now. SemiAccurate's sources say that Granite has now been pushed back**  
21 **to 2H 2023 which is where [Granite Rapids' successor] Diamond Rapids was set to**  
22 **debut as of last week.**

24 <sup>28</sup> Charlie Demerjian, *Nvidia, AMD, and VIA quit BAPCO over SYSmark 2012*, SemiAccurate  
25 (June 20, 2011), <https://semiaccurate.com/2011/06/20/nvidia-amd-and-via-quit-bapco-over-sysmark-2012/>.

26 <sup>29</sup> See Charlie Demerjian, *Nvidia's 28nm mobile lineup leaked*, SemiAccurate.com (Aug. 23, 2011),  
27 <https://semiaccurate.com/2011/08/23/nvidias-28nm-mobile-lineup-leaked/>.

28 <sup>30</sup> See Charlie Demerjian, *AMD's 28nm mobile lineup leaked too*, SemiAccurate.com (Aug. 24, 2011),  
<https://semiaccurate.com/2011/08/24/amds-28nm-mobile-lineup-leaked-too/>.

1       **This means Intel just pushed out their server roadmap a full generation.** Given how  
2 far behind AMD that Intel is right now, it is hard to see why this roadmap makes any sense  
3 at all. **The first time Intel could have been in the same ballpark with AMD was pushed**  
4 **out by a full generation. If this doesn't seem scary to you, consider this, Intel's first**  
5 **7nm server part is Granite Rapids.**

6       **Intel repeatedly claims we will see 7nm server CPUs in 2021 but their roadmaps**  
7 **unquestionably say that is late 2023. Either Intel's top management is so untethered**  
8 **from what is happening at the engineering level or someone is bending the facts to a**  
9 **very scary degree.** What this means is that as long as both sides execute on their  
10 roadmaps, Intel will now not reach parity with AMD until 2H23 best case but more  
11 realistically on the next platform 5-6 quarters later.

12       **Although SemiAccurate has been researching why things are getting progressively**  
13 **worse at Intel, we don't have a clear answer. Things have been slipping for so long**  
14 **now, interrupted by the occasional big slide, it looks cultural.** Given the 3-4 year time  
15 frame to make a new server platform from scratch, does it make sense to keep sinking the  
16 effort in to something you know won't come close to the competition?

17       78.     Thus, in contrast to Intel's public assurances, Intel's 7 nm process was far from "on track"  
18 from the beginning of the Class Period, as reflected in the December 12, 2019 SemiAccurate article.  
19 Accounts from former Intel employees corroborate SemiAccurate's report of a significant delay in 7 nm  
20 manufacturing. For example, facts reported by FE 1, a Senior Director of Marketing at Intel from April  
21 2018 until December 2019, demonstrate that, no later than December 2019, it was understood that the  
22 7 nm would be significantly delayed. FE 1 reported into Raja Koduri, Chief Architect at Intel, spent a  
23 lot of time with him, and said it was understood during FE 1's time at Intel that "yea, 7nm is messed up."  
24 FE 1 relayed that at some point before FE 1 left Intel in December 2019, Jon Carvill ("Carvill"), a former  
25 Vice President of Marketing at Intel, told FE 1 that things were 1-2 years behind with the 7nm. FE 1  
26 explained that Carvill possessed accurate information about the delay because Carvill was in charge of  
27 marketing transistors and memory; therefore, Carvill spent a lot of time with the manufacturing group in  
28 order to understand the current state of affairs so that he could articulate the status to customers.  
According to FE 1, it was reasonable to believe the Company knew in the tail end of last year (i.e., 2019)  
that they were not going to turn things around.

79.     FE 2, was an Intel employee from May 1993 until September 2020, including working as  
a Development Technician at the Aloha campus in Aloha, OR, and as an Operations Manager at Intel's  
Ronler Acres campus in Hillsboro, OR. FE 2 reported that Intel employees knew that 7 nm was not



1 yielding as it should be and that it was rare to see anything yield past one or two die. FE 2 emphasized  
2 that yielding issues are immediately apparent because “as soon as they [the technicians] run their test, we  
3 know.”

4 **2. Nevertheless, Defendants Continue to Falsely Reassure Investors**  
5 **that the 7 nm Process Remains “on Track”**

6 80. Notwithstanding the facts set forth above, throughout the Class Period, Defendants  
7 continued to repeat their statements that Intel’s 7 nm process was “on track” to launch in 2021 with a full  
8 suite of CPU products in 2022. For instance, during Intel’s January 23, 2020 Q4 2019 earnings call—  
9 well after Intel had already altered its internal product roadmaps by shifting its 7 nm timeline out a full  
10 year—Swan emphasized during his prepared remarks that “[o]ur 7-nanometer process remains on track  
11 to deliver our lead 7-nanometer product, Ponte Vecchio, at the end of 2021, with CPU products following  
12 shortly after in 2022.” Swan also answered an analyst’s question by stating that “our expectations is  
13 we’ll have our first 7-nanometer product launched in the latter part of 2021 with CPUs to closely  
14 follow . . . we’ll ramp 7 on a 2-year cadence in 2021.”

15 81. These statements continued to sway the market. Reacting to Swan’s January 23, 2020  
16 comments, UBS analysts reported that same day that “there was no wavering on 10/7nm timelines” and  
17 raised their price target from \$60.00 to \$75.00 per share. The next day, January 24, 2020, J.P. Morgan  
18 analysts wrote that “the [Intel] team remains on track for its first 7nm products (Ponte Vecchio) in 2021,”  
19 rated the stock “Overweight,” and raised their price target from \$68.00 to \$80.00 per share. That same  
20 day, Morgan Stanley analysts raised their price target to \$71.00 per share, rated Intel’s stock  
21 “Overweight,” and noted that “[i]t’s going to be important for the company to execute to its roadmaps  
22 across 14 nm, 10 nm+, and 7 nm in late 2021 . . . .” Intel’s common stock opened the next day (January  
23 24, 2020) at \$66.57 per share, up \$3.25 (5.13%) over the prior day’s closing price and went on to finish  
24 that day’s trading at \$68.47, up \$5.15 (8.13%) over the prior day’s closing price.

25 82. At no point during the next six months did Defendants waver in their public confidence  
26 in the Company’s 7 nm roadmap. For example, while representing Intel at the Morgan Stanley  
27 Technology, Media & Telecom Conference on March 2, 2020, Defendant Davis addressed an analyst’s  
28 question about “the progress of 10-nanometer and 7-nanometer and your confidence level going forward

there?” Davis responded that Intel still “expect[ed] to start the 7-nanometer period . . . at the end of ‘21,” and that “we feel like we’re starting to see the acceleration on the process side that we have been talking about to get back to parity in the 7-nanometer generation and regain leadership in the front down there.”

83. Analysts and the market were buoyed by Davis’s statements. For example, that same day BofA Securities (“BofA”) analysts wrote that Intel was “well on its way to working through past issues” and that “management already has its sight set on transitioning to what it expects to be a more productive/performant 7nm node by the end of 2021,” rated Intel’s stock “BUY” and gave it a “Price Objective” of \$75.00. The same day, Wells Fargo analysts reported that “Mr. Davis . . . noted that Intel is focused on . . . achieving parity at 7nm node and then regaining leadership in subsequent 5nm . . . focus on fast move to 7nm process node into 2021 (led with data center GPUs; *Ponte Vecchio*) – emphasizing confidence in where Intel is going on their roadmap,” and assigned a price target of \$70.

**3. On March 31, 2020, Intel Misses Its Hard Tapeout Deadline for Its First 7 nm Product (Ponte Vecchio), Yet Defendants Continue Falsely Reassuring Investors that the 7 nm Process Is “Well on Track”**

84. “Tapeout” of a chip is the step in the manufacturing process when the manufacturing specifications are completed and sent to the fab to begin the actual manufacturing process. Although interim tapeout deadlines can be missed if the chip’s design or manufacturing recipe is simply not yet ready (or if the manufacturing process is not yet developed enough to fabricate it), and slack is often built into the development process to account for such slippage, a “hard” tapeout deadline is the last such date a chip can be taped out to avoid a cascading series of wider delays to the rest of the manufacturing timeline.

85. As described above in Parts I and IV.C, Ponte Vecchio was Intel’s first 7 nm product, its first 7 nm datacenter GPU, a “halo” product for Intel’s process node advancements, and the key component of Intel’s Aurora supercomputer project for the DOE. In short, it was critical that Intel meet the hard tapeout deadline for this product in order to have any chance to satisfy its publicly-announced deadline for the 7 nm launch.

86. Intel failed to meet its hard tapeout deadline for Ponte Vecchio. According to a SemiAccurate article published on July 24, 2020 (after one of the corrective disclosures in this case),

1 “[t]here was an internal mandate to tape the chip out before the end of Q1/2020 [i.e., March 31, 2020] or  
2 heads would roll, anything later and the Aurora contract would be missed and Intel would get a big,  
3 expensive, and public black eye. They missed the tapeout date. Heads rolled.”<sup>31</sup> SemiAccurate  
4 concluded, therefore, that Intel “knew the delays to 7nm when they missed their hard tapeout deadline  
5 for the first 7nm product, Ponte Vecchio, on March 31, 2020 . . . .”<sup>32</sup>

6 87. Taping out Ponte Vecchio after March 31, 2020, meant Intel’s contractual roadmap for  
7 Project Aurora was jeopardized. Moreover, as Renduchintala had explained on December 10, 2019, Intel  
8 had chosen Ponte Vecchio, a GPGPU, to be Intel’s “lead vehicle for 7 nanometer” instead of a CPU  
9 because a “GPGPU by nature of its architecture and redundancy in the architecture makes it a lot more  
10 amenable to being a good ramp vehicle in the early phases of a new node . . . .” In short, the fact that  
11 Ponte Vecchio had still not yet taped out by the end of March 2020 meant not only that Ponte Vecchio,  
12 but Intel’s entire 7 nm process node effort (including any subsequent 7 nm CPUs) was significantly off  
13 track and behind schedule.

14 88. Nevertheless, Defendants continued to falsely reassure the market otherwise. Having  
15 missed Ponte Vecchio’s hard tapeout deadline on March 31, 2020, Swan and Davis were notably silent  
16 in their prepared remarks at the beginning of Intel’s April 23, 2020 Q1 earnings call regarding the status  
17 of 7 nm. Although neither Swan nor Davis volunteered any update on 7 nm, analysts requested one  
18 during the question-and-answer portion of the call. Neither Swan nor Davis came clean when asked  
19 about this subject. In response to one analyst’s question about the 7 nm status, Swan stated that “we plan  
20 to get back on a 2- to 2.5-year cadence, which means in 2021, we’ll be ramping 10-nanometer even more  
21 while we’re investing in 7-nanometer that we anticipate having in the fourth quarter of 2021.” Swan then  
22 emphasized that “*we’re well on track from the plans we laid out . . . .*”

23 89. Analysts responded positively to this news. On April 24, 2020, J.P. Morgan analysts  
24 wrote that “the [Intel] team remains on track for its first 7nm products in 2021” and “[t]he team is  
25

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26 <sup>31</sup> Charlie Demerjian, *What is going on with Intel’s Ponte Vecchio GPU?*, SemiAccurate (July 24,  
27 2020), <https://semiaccurate.com/2020/07/24/what-is-going-on-with-intels-ponte-vecchio-gpu/>.

28 <sup>32</sup> Charlie Demerjian, *An examination of Intel’s 7nm timeline delay claims*, SemiAccurate (July 24,  
2020), <https://semiaccurate.com/2020/07/23/an-examination-of-intels-7nm-timeline-delay-claims/>.

executing well on its product/manufacturing roadmaps . . . .” That same day, analysts at UBS wrote that “[b]ottom line, we remain bullish here as . . . the manufacturing narrative is about to gain significant momentum” and “the main fulcrum on the investment case remains [Intel’s] progress in catching up to TSMC (and, ergo, AMD) on manufacturing and we would argue that the read through was, if anything, better as . . . 7nm remains totally on track.”

**4. In May 2020, Slides of Intel’s Internal Roadmap Further Confirm that Its First 7 nm Server CPU Products Are a Year Behind Their Publicly-Announced Launch Date**

90. On June 3, 2020, a series of leaked Intel slides (in English but partly in Russian) dated “May 2020” was posted on Twitter:<sup>33</sup>

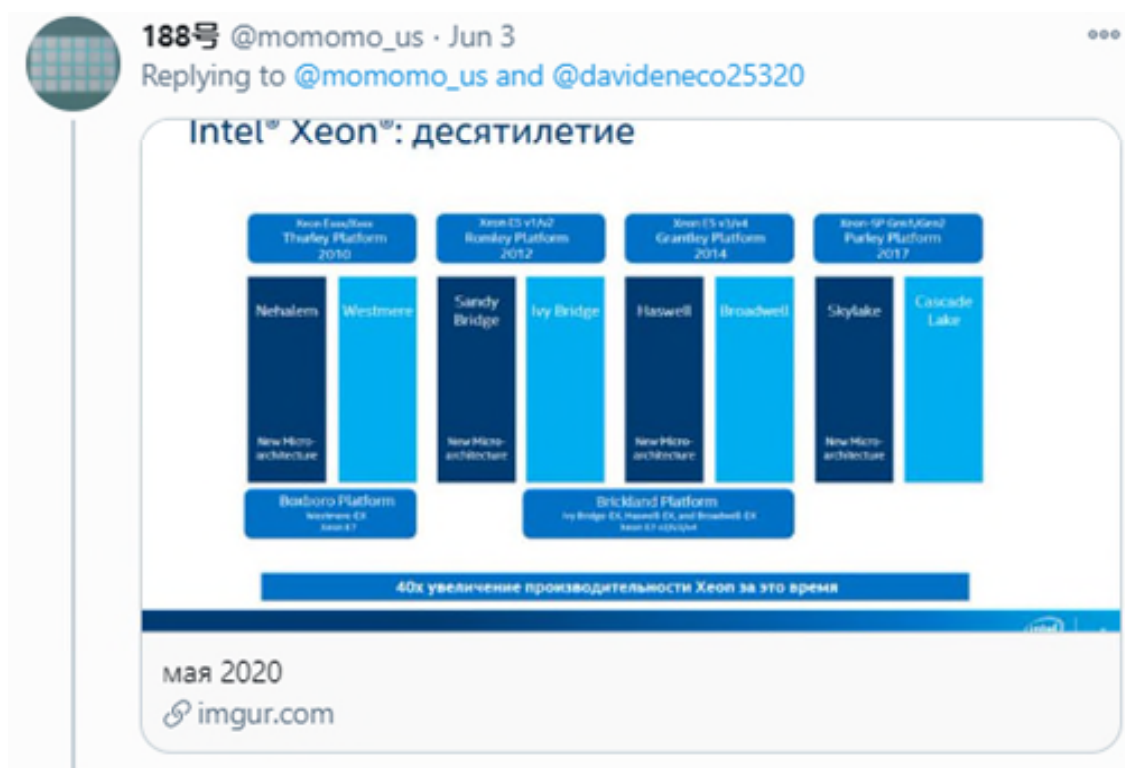


Figure 7: June 3, 2020 Twitter post of leaked slide from Intel Russia dated “мая 2020” (May 2020).

<sup>33</sup> As set forth on the slide, “мая” is the genitive declension of “май,” which is Russian for the month of “May.” Hence, the June 3, 2020 Twitter post states, in correct Russian grammar, that these slides are dated “May 2020”. See [https://web.archive.org/web/20201222183246/https://twitter.com/momomo\\_us/status/1268148786875887616](https://web.archive.org/web/20201222183246/https://twitter.com/momomo_us/status/1268148786875887616). The slides were simultaneously posted to <https://imgur.com/a/fq7bTFe> (stating “мая 2020”).

91. On June 6, 2020, *WCCFtech*, “a leading technology publication house,”<sup>34</sup> published an article reposting the same slides.<sup>35</sup> One slide, titled “Intel® Xeon®: the Present,”<sup>36</sup> provided a roadmap for Intel’s Xeon server CPU products. As depicted below, the roadmap shows Intel’s 10 nm “Sapphire Rapids” server CPU arriving in the first half of “2023” and the “Next Gen” server CPU products arriving after “Sapphire Rapids” in the second half of “2023”:

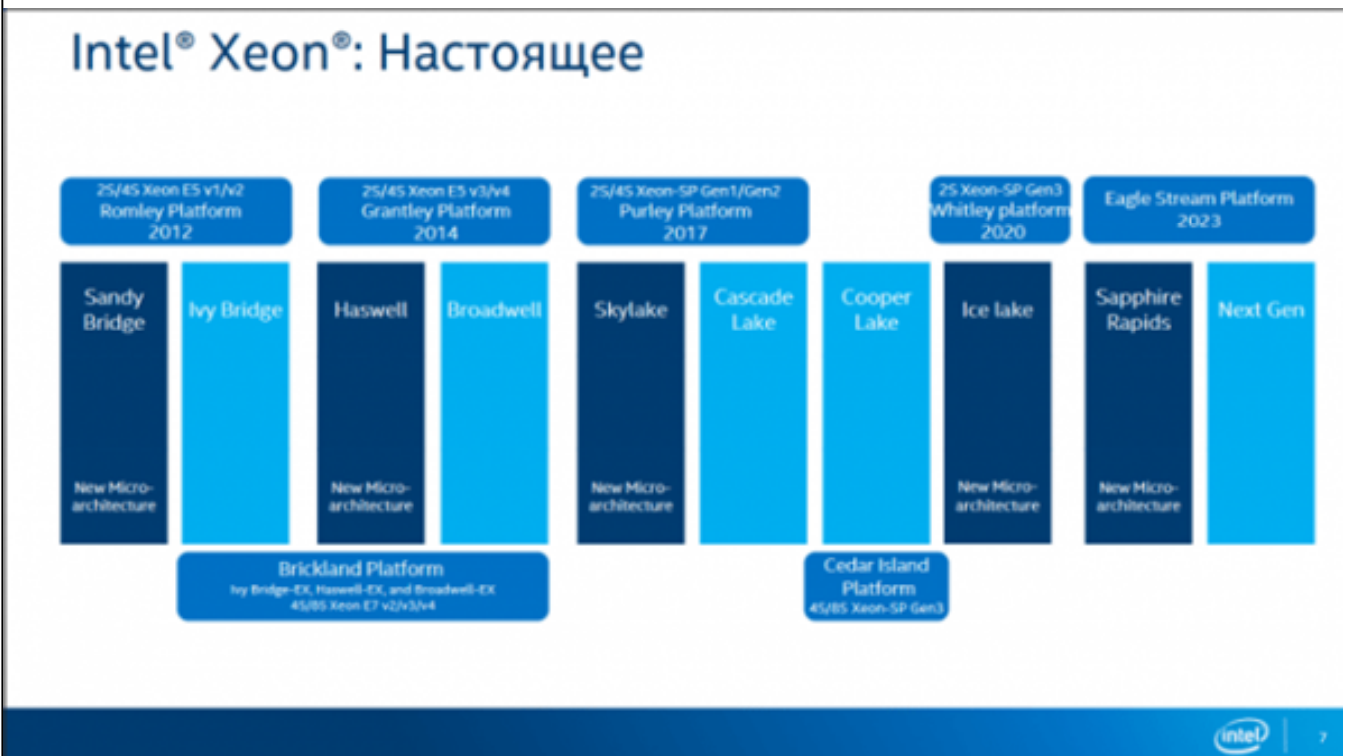


Figure 8: Leaked slide from Intel Russia depicting Intel’s 10 nm “Sapphire Rapids” server CPU products arriving in the first half of “2023” and the “Next Gen” server CPU products arriving after “Sapphire Rapids” in the second half of “2023.”

<sup>34</sup> See <https://wccftech.com/about/>.

<sup>35</sup> See Hassan Mujtaba, *Intel 10nm Sapphire Rapids Xeon Scalable Family With DDR5 & PCIe 5.0 Coming 2021, Will Compete Against AMD’s EPYC Genoa ‘Zen 4’ Server Chips*, WCCFtech (June 6, 2020) (“In a leaked roadmap from Intel Russia which was spotted by Momomo\_US a few days ago, we get to see some more information on where the Intel Xeon Scalable Family is headed with its next-generation Eagle Stream Platform which will support 2 major Xeon families, Sapphire Rapids & Granite Rapids.”). Intel’s operations in Russia are known as “Intel Russia” (see <https://blogs.intel.com/jobs/2020/09/the-keys-to-success-at-intel-russia/#gs.o7k8c2>) or “Intel in Russia” (see <https://www.intel.com/content/www/us/en/jobs/locations/russia.html>).

<sup>36</sup> “Intel® Xeon®: Настоящее” translates to “Intel® Xeon®: the Present.”

1           92. In discussing the above roadmap, the *WCCFtech* article noted that “[i]n its roadmap, Intel  
2 also shows that Sapphire Rapids will bring a new architecture which is hinted by the dark blue color that  
3 refers to a Tock while Granite Rapids would bring forth a smaller process node, also referred to as a Tick  
4 and hinted by light blue color.” The “smaller process node” that “Granite Rapids would bring forth,” of  
5 course, was 7 nm. These leaked slides of Intel’s product roadmap further confirmed that Intel’s 7 nm  
6 server CPU was not slated to come to market until the second half of 2023, far past the 2022 roadmap  
7 that Defendants assured investors Intel was on track to meet. Notwithstanding this fact, Defendants  
8 continued to falsely reassure investors through June 2020 that Intel remained on track with its 7 nm  
9 process timeline, as set forth in Section VI below.

10                   **5. In May or June 2020, Keller Told the Board that Swan and**  
11                   **Renduchintala Should Be Removed for, Among Other Things, the**  
12                   **Failure of the 7 nm Process**

13           93. By approximately May or June 2020, the systemic 7 nm delays had sown internal strife  
14 among Intel’s senior executives, including between Keller – the renowned chip architect – and his boss,  
15 Defendant Renduchintala. According to FE 1, who was informed of these events by Carvill, the former  
16 Vice President of Marketing discussed above at ¶ 78, Keller approached Defendant Swan around this  
17 time to tell Swan that Renduchintala was not addressing the problems causing the 7 nm delays because  
18 Renduchintala was too afraid to lose support from Intel’s foundries and their workforce. FE 1 said Carvill  
19 stayed very close to both Raja Koduri and Keller even after Carvill left Intel. FE 1 stated that  
20 Renduchintala’s refusal to address the known problems with 7 nm upset Keller to such a degree that  
21 Keller threatened to resign if Swan did not make the changes Keller wanted. According to FE 1, Keller’s  
22 plea and threat to resign fell on Swan’s deaf ears.

23           94. Yet, as FE 1 explained, Swan’s refusal to engage did not deter Keller. Indeed, FE 1 said  
24 that Keller went directly to the Intel Board of Directors and informed them that neither Renduchintala  
25 nor Swan should remain in their roles. FE 1 said that Keller’s embarrassment of Swan in front of the  
26 Intel Board of Directors prompted Keller’s abrupt departure from the Company in mid-June.  
27  
28

V. AS THE TRUTH WAS GRADUALLY REVEALED, DEFENDANTS CONTINUED TO MISLEAD THE MARKET REGARDING 7 NM

A. On June 11, 2020, Intel Announces Keller's Surprise Resignation, But Again Falsely Reassures Investors that the 7 Nanometer "Timeline Remains Unchanged"

95. On June 11, 2020, following the market's close, Intel announced Keller's abrupt and immediate resignation due to unspecified "personal reasons," though Keller agreed to "serve as a consultant for six months to assist with the transition." Media reports indicated that, since Keller's hiring he had been "streamlin[ing] a lot of the product development process on the silicon side" as well as "providing strategic platforms through which future products can be developed and optimized to market," and "had a hand in looking at Intel's manufacturing processes, as well as a number of future products."<sup>37</sup> With respect to the future products, Keller was purportedly "overseeing" a "massive chip redesign" for Intel, which would involve "cleanly separat[ing] major functions, to make it easier for the company to improve one section at a time," reminiscent of the disaggregated "chiplet model Keller used at AMD" for its Zen architecture which, as described above in Section IV.B, was now competitively positioned to eat away at Intel's market share.<sup>38</sup> Along with Keller's sudden departure, Intel revealed significant leadership changes within TSCG—the group responsible for engineering and manufacturing Intel's semiconductor chips, including its 7 nm technology.

96. The abruptness of Keller's departure combined with the shortness of his tenure led to skepticism on the part of both analysts and the media, who questioned the public explanation, and reported that his departure hinted that Intel's processor and process node roadmaps were in trouble. For example, in a note issued on June 11, 2020, Rosenblatt Securities observed that the departure of Intel's "rock star processor architect and SVP of Silicon Engineering Jim Keller . . . is a big deal and suggests that whatever he was implementing at Intel was not working or the old Intel guard did not want to implement it." Rosenblatt also noted that "Mr. Keller ha[d] a rich record of accomplishments at

<sup>37</sup> See Dr. Ian Cutress, *Jim Keller Resigns from Intel, Effective Immediately*, AnandTech (June 11, 2020), <https://www.anandtech.com/show/15846/jim-keller-resigns-from-intel-effective-immediately>.

<sup>38</sup> See Aaron Pressman, *Why Intel is betting its chips on microprocessor mastermind Jim Keller*, Fortune (May 18, 2020), <https://fortune.com/longform/microchip-designer-jim-keller-intel-fortune-500-apple-tesla-amd/>.

1 AMD . . . , Apple . . . , and Tesla . . . , with Intel hiring him to streamline, align, and really fix the  
2 microarchitecture and manufacturing process roadmaps. . . . *[T]he net of this situation for us is that*  
3 *Intel’s processor and process node roadmaps are going to be more in flux or broken than even we had*  
4 *expected.*” Bernstein analysts noted that “resigning for ‘personal reasons’ leaves things open to  
5 considerable speculation; given the suddenness it does not necessarily have a ‘planned’ flavor to it.”

6 97. Despite these drastic changes, Intel reassured investors that its chip engineering and  
7 manufacturing group remained strong and that its 7 nm development was on track under Renduchintala’s  
8 leadership. Intel’s June 11, 2020 release announcing Keller’s resignation touted the Company’s “vastly  
9 experienced team of technical leaders within its Technology, Systems Architecture and Client Group  
10 (TSCG) under the leadership of Dr. Venkata (Murthy) Renduchintala, group president of TSCG and chief  
11 engineering officer.”

12 98. Moreover, earlier on June 11, 2020, ahead of the Keller announcement, Swan and Davis  
13 met with analysts from Deutsche Bank and emphasized, among other things, Intel’s 7 nm progress.  
14 Deutsche Bank reported that Intel was “[l]ooking forward to 7nm” and that its “time-line remains  
15 unchanged with a late 2021 launch targeted (Datacenter GPU initially) and 2022 volume ramps in CPUs  
16 (both server/PCs).”

17 99. Swan and Davis’s reassurances on June 11, 2020 that Intel’s “7nm . . . time-line remains  
18 unchanged” buffered market reaction to the news of Keller’s sudden departure. Intel’s stock price  
19 declined by 0.6%, or \$0.37 per share, from a closing price of \$59.70 per share on June 11, 2020 to a  
20 closing price of \$59.33 per share on June 12, 2020.

21 100. Throughout June, Defendants continued to reassure the market that all was well with  
22 Intel’s 7 nm. For instance, on June 25, 2020, *Consumer Electronics Daily* published an article stating  
23 that “[a]n Intel spokesperson emailed Wednesday [i.e., June 24, 2020] that its 7-nanometer process  
24 ‘remains on track’ with first products due by the end of 2021.”

25 **B. On July 23, 2020, Intel Belatedly Reveals that Its 7 nm Process Is**  
26 **Substantially Delayed**

27 101. Only weeks after assuring investors that the 7 nm timeline remained unchanged,  
28 Defendants shocked the market by admitting that Intel’s 7 nm process was, in fact, substantially delayed.



1 On July 23, 2020, after the market had closed, Intel issued a press release announcing the Company's  
2 Q2 2020 financial results, which beat Wall Street's expectations in most respects. Both revenue and  
3 earnings were up double-digit percentages year-over-year, with revenue growth in Intel's critical DCG  
4 and CCG business units helping set record earnings for the Company. However, amidst these positive  
5 financial results, the release also stated that Intel's "7nm product transition [was] delayed versus prior  
6 expectations." The press release elaborated: "The company's 7nm-based CPU product timing is shifting  
7 approximately six months relative to prior expectations" and "[t]he primary driver is the yield of Intel's  
8 7nm process, which based on recent data, is now trending approximately twelve months behind the  
9 company's internal target."

10 102. During Intel's Q2 earnings call later that day, Swan provided additional details regarding  
11 these bombshell revelations. Swan stated that a "defect mode . . . that resulted in yield degradation" was  
12 the cause of the significant 7 nm delay, and while he asserted that Intel had "root caused the issue, and  
13 believe[d] there are no fundamental roadblocks," he did not provide additional detail regarding the nature  
14 of the defect, when it was discovered, whether Intel had identified a fix, or the basis for the extended  
15 delay. Swan also disclosed that Intel "now expect[s] to see initial production shipments of our first Intel-  
16 based 7-nanometer product, a client CPU, in late '22 or early '23," thus backtracking on earlier assurances  
17 that (after Ponte Vecchio) its first 7 nm products would be its critical data center CPU products.<sup>39</sup> Now,  
18 those 7 nm data center CPUs would not "see initial production shipments" until "the first half of '23."

19 103. As if the delay was not enough, Swan also disclosed that Intel was going to utilize an  
20 outside manufacturer to make some of its leading-edge 7 nm chips. This step was unprecedented in  
21 Intel's history. It revealed that Intel's ability to manufacture its 7 nm process was so severely deficient  
22 that it had to outsource the production of its leading-edge technology to a rival, which represented a  
23

24 <sup>39</sup> Earlier discussions of Intel's 7 nm roadmap had emphasized that Ponte Vecchio would be  
25 followed next by 7 nm server chips, with CCG chips for consumer and commercial laptop and desktop  
26 computers following last. *See, e.g.*, ¶ 63 (Renduchintala: "The next product on 7-nanometer will be a  
27 data center CPU. . . . [A] data center GPGPU [Ponte Vecchio] followed by a data center CPU is the way  
28 we're planning the road map."). This roadmap reversed Intel's longstanding historical practice (which  
had been followed through 10 nm), of first ramping "small core" chips for its CCG business, followed  
by a months-long delay before ramping its "large core" server chips for DCG. This roadmap reversal  
reflected the importance of getting DCG's high-margin (but lower yielding) data center products, which  
were critical to the Company's bottom line, to the market as soon as possible.

1 severe blow to the Company's defining IDM business model. Specifically, Swan disclosed that "our data  
2 center GPU design, Ponte Vecchio, will now be released in late 2021 or early 2022, utilizing *external*  
3 *and internal process technologies*, combined with our world-leading packaging technologies."

4 104. Swan's remarks also made clear that Intel had been preparing to take this unprecedented  
5 step for far longer than it had disclosed to investors. Specifically, Swan explained that another  
6 (previously undisclosed) "lesson" that Intel learned from the 10 nm experience was that the Company  
7 needed "contingency plans" to "leverage somebody else" to manufacture its 7 nm process, particularly  
8 its Ponte Vecchio chip:

9 And I think the importance of our many lessons coming out of 10-nanometer, one of them  
10 was how do we ensure that we have contingency plans in the event that our advancements  
11 in process technology, as it gets increasingly complicated, do not play out the way we'd  
12 hope . . . . [W]hat's different is we're going to be pretty pragmatic about if and when we  
13 should be making stuff inside or making outside and making sure that we have optionality  
14 to build internally, mix and match inside and outside or go outside in its entirety if we need  
15 to. And that's kind of one of our learnings coming out of 10 is, in the event process doesn't  
16 move along as we expect, let's make absolutely sure, with advanced contingency planning  
17 and real milestones, that we can glitch the best we can to leverage somebody else and not  
18 slip product schedules in light of process complexities.

19 105. This was the first time that Intel investors were made aware that the Company had any  
20 "contingency plans" to outsource one of its leading-edge chips—a significant departure from Intel's past  
21 practices and Defendants' repeated statements about the Company's competitive IDM advantage.

22 106. In contrast to the announced 12-month delay for Intel's own 7 nm process, Intel projected  
23 a smaller delay for Ponte Vecchio of either "late 2021" or "early 2022." However, this would only be  
24 possible if Intel had already missed enough internal development milestones to warrant outsourcing Ponte  
25 Vecchio's design to another fab (such as TSMC) long before July 23, 2020. Many months of significant  
26 reengineering work would have been required to allow the Ponte Vecchio design to be fabricated on  
27 another fab's process rather than at Intel's internal 7 nm fab. In this respect, FE 3, a former Intel circuit  
28 design engineer at its Hillsboro, Oregon location from approximately 2005 until March 2020, stated that  
that there would be a significant amount of redesign work to do manufacturing at TSMC. FE 3 confirmed  
that if you wanted to covert the design for Intel's 7nm to another company, it would be a significant  
undertaking, even more so when you are talking about a different company with a completely different  
approach to the manufacturing process, such as TSMC. FE 3 estimated that such work was a "major"

1 thing and would take at least “eight months” or “a year” to complete. Indeed, later during the call, Swan  
2 responded to an analyst’s question by admitting that “for the last couple of years, with the real focus on  
3 product leadership . . . *[w]e’ve been designing our products* and advancing our packaging technology so  
4 that we have much more flexibility to decide if and when we will use our fabs *or somebody else’s* to  
5 deliver that annual cadence of leadership products.” This disclosure, which Swan attempted to spin as a  
6 positive, for the first time confirmed that for years Intel had been designing its leading-edge chips for  
7 potential manufacture by external foundries.

8 107. Following these revelations, throughout the question-and-answer portion of the call,  
9 analysts ignored almost entirely the Company’s positive Q2 financial results and were instead focused  
10 on the newly disclosed 7 nm delays and the resulting competitive and financial implications. The first  
11 analyst to speak observed that “on the competitive side, by the time you come out with 7 [nm], TSMC is  
12 planning to be on the 3-nanometer node so will still be a generation ahead” and asked “what’s the market  
13 share implication of that?” Another analyst questioned Intel’s “confidence level . . . that this is sort of a  
14 one-and-done issue and it doesn’t turn into a repeat of 10 [nm] where you kind of had multiple periods  
15 of pushouts,” which, as another analyst put it, “frustrated [investors] with how long the misexecution on  
16 the manufacturing has happened.” Other analysts followed suit, asking questions that probed the negative  
17 implications of the 7 nm delay and the fundamental shifts from the Company’s IDM business model that  
18 the outsourcing of its leading-edge products would entail. In concluding the call, Swan stated “we feel  
19 pretty good about where we are, though we’re not happy. I’m not pleased with our 7-nanometer process  
20 performance.”

21 108. The response from the analyst community was immediate and overwhelmingly negative.  
22 On July 23, 2020, Deutsche Bank wrote “[m]ore manufacturing missteps move us to sideline,” lowered  
23 its price target from \$70.00 to \$60.00, and downgraded the stock “from Buy to Hold,” noting that “delays  
24 in [Intel’s] 7nm process node” was “by far the biggest factor that will pressure the stock as investors will  
25 fear the duration of 7nm delays could be longer (ala 10nm) and that [Intel] is falling further behind  
26 TSMC.” On July 23, 2020, Credit Suisse analysts wrote a report titled “Tantalus, Sisyphus and Intel . . .”  
27 in which they lowered their target price for the stock from \$75.00 to \$70.00 and commented that “the  
28 execution shortfall on 7nm on the heels of the Jim Keller resignation, will re-ignite concerns on

1 competitive position which will be difficult to refute and is a risk – the easy defensible narrative is  
2 [Intel’s] results are bullish for AMD . . . .”

3 109. Also on July 23, 2020, Rosenblatt Securities published a report observing that “the 7nm  
4 process ramp delay into 2023, and clear shift to a foundry easy-button option will set the stage for a lively  
5 debate on the merits of the company’s business model and likely share losses for years to come. We  
6 think Keller’s recent departure from Intel is just the tip of the iceberg . . . a chaotic situation that we sense  
7 will not play well with customers. . . . The notion of Intel as a fabless or fab lite company may be helpful  
8 at some point, but it clearly eliminates the historical and fundamental Intel advantage of 2-year global  
9 process technology leadership.” Rosenblatt maintained its “Sell” rating on Intel stock, which it believed  
10 “warranted due to the change in the business model, suspect secular sales growth, sub-optimal  
11 manufacturing (lagging leading foundries by 1-2 years), delayed/broken new adjacency growth vectors,  
12 and share losses in CPUs that are expected to be multi-year in nature.”

13 110. That same day, *Bloomberg* also published an article stating that “the worst fears over  
14 Intel’s pipeline is now realized.”<sup>40</sup>

15 111. Also that day, Cowen analysts also published a report titled “Yes, It’s that Bad; with  
16 TSMC Humming Along, 7nm Couldn’t Afford to Be Pushed,” observing that “Intel’s 2Q beat was  
17 completely overshadowed by a 6-month 7nm CPU pushout on a 12-month manufacturing delay.” The  
18 next day, July 24, 2020, the market continued to digest and react to Intel’s announcement of its delayed  
19 7 nm process, including Defendants’ comments to analysts during the July 23, 2020 Q2 earnings call  
20 after the market had closed. Bernstein analysts wrote that Intel’s Q2 earnings call was “the worst we  
21 have seen in our career covering the company” and “[f]rom here we see things growing increasingly  
22 painful as 7nm delays are likely to overshadow anything good they [Intel] can put forth, while magnifying  
23 any negative events, all while they fight an existential conflict with themselves as they attempt to figure  
24 a way out of the hole they have dug.” Despite Intel’s record financial results, the analysts wrote that  
25 “frankly, none of the numbers matter” and “investors could have stopped reading the press release after  
26

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27 <sup>40</sup> See Tae Kim, *Intel Just Gave Investors Even More Reasons to Worry*, Bloomberg News  
28 (July 23, 2020), <https://www.bloomberg.com/opinion/articles/2020-07-23/intel-earnings-chip-delay-gives-investors-more-reason-to-worry>.

1 the fourth line on the first page, which indicated Intel delaying their 7nm trajectory with yields running  
2 a year behind internal targets, and with the CPU roadmap (originally slated for mid-2022) pushed by 6  
3 months to the end of 2022 or start of 2023. . . . And the set-up from here appears extremely challenging,  
4 with tough compares, continuing share losses (both to AMD and, now, AAPL), margin compression, and  
5 **a complete loss of credibility** on top of process headwinds.” The analysts added, “While Intel suggested  
6 they at least know what the problem is, **it certainly doesn’t sound like a fix is forthcoming anytime soon**  
7 given the magnitude of the delay and Intel’s potential solution, namely, to possibly give up and embrace  
8 a much larger outsourcing strategy. . . . [W]e are back to square one, with Intel’s process deficiencies  
9 now growing wider than ever,” and wrote, “**any shreds of credibility this management team might have**  
10 **had have now gone out the window.**” The report concluded that “[t]he risk-reward on the stock . . .  
11 seems to be to the downside, even following a likely sharp move south to come today.” Accordingly,  
12 Bernstein lowered its “target price to \$45” and “downgrade[d] Intel to Underperform.”

13 112. On July 24, 2020, Raymond James analysts wrote that “[w]e view the roadmap missteps  
14 to be [a] stunning failure for a company once known for flawless execution, and could well represent the  
15 end of Intel’s computing dominance.” That same day, in a report titled “Heresy No More,” BMO Capital  
16 Markets published the following: “After delays in its 10-nm manufacturing process node, [Intel] stat[ed]  
17 not that long ago that it would regain the normal Moore’s Law cadence when on 7-nm.” But, “Intel  
18 dropped a bombshell by [disclosing] a 12-month process delay/6-month product delay on its 7-nm  
19 process. . . . Not that long ago, Intel and manufacturing prowess were synonyms. No more.” BMO then  
20 presciently observed that “the unthinkable may not be that far away when Intel is forced to acknowledge  
21 that the growing gap between it and the TSMC camp is an insurmountable chasm, and outsource key  
22 parts of its manufacturing/process technology.”

23 113. That same day, Susquehanna published an article titled “Intel Corporation: It’s Time to  
24 Sell Your Fabs to TSMC!” deeming the 7 nm delay a “dropped bomb” and “mistake [Intel] can’t afford  
25 after the slippery slope that was 10nm.” The Susquehanna report concluded that “[w]ith this latest push-  
26 out of process technology, we believe Intel has zero-to-no chance of catching/surpassing TSM (AMD  
27 partner) . . . at least for the next half decade, if not . . . ever.”  
28

1           114. Also that day, Morgan Stanley analysts wrote that “7 nm delays are a negative,” noting  
2 that “[Intel] said that [its] first 7 nm product would be a client microprocessor in ‘late 2022 or early 2023’,  
3 whereas at the analyst day last year they had talked about the first 7 nm product as the Ponte Vecchio  
4 GPU in 4q21 (without providing a timeline for microprocessors). And the implication is that 7 nm  
5 Granite Rapids (the first server chip on the process) would come even later, perhaps in mid 2023.” The  
6 report further noted that Intel’s “willingness to outsource shown on [the] call can be interpreted  
7 negatively,” and that “the clearly articulated plan to use foundry as a ‘contingency plan’ for  
8 microprocessors is a new direction for the company.” Regarding the delay of Granite Rapids, the report  
9 further noted that “server products are obviously critical. It would appear that the company does not have  
10 a product refresh in 2022, with Sapphire Rapids on track for 2h21, and the 7 nm follow on [i.e., Granite  
11 Rapids] likely in mid 2023.” Notably, this timing for Granite Rapids is what SemiAccurate reported  
12 Intel’s internal roadmaps showed *no later than December 2019*.

13           115. Also on July 24, 2020, Barclays analysts commented, “We believe Intel has already  
14 shifted its DC GPU [i.e., Ponte Vecchio] to TSMC, but we believe it is not possible for Intel to shift any  
15 material CPU volumes to TSMC as they simply don’t have the leading edge capacity and we see little  
16 chance of TSMC buying Intel’s fabs.” Barclays lowered its price target for Intel’s stock from \$58.00 to  
17 \$48.00 per share.

18           116. As a result of these disclosures, Intel’s stock price declined by \$10.83 per share, or  
19 **17.93%**, from a closing price of \$60.40 per share on July 23, 2020, to a closing price of \$49.57 per share  
20 on July 27, 2020.

21           117. On July 27, 2020, Intel issued a press release announcing a substantial reorganization of  
22 the Company’s TSCG group, including the unplanned departure of Renduchintala.

23           118. Analysts reacted to Renduchintala’s departure as an implicit admission of the crisis Intel  
24 faced as a result of the 7 nm delays. For example, the same day, Rosenblatt Securities published an  
25 analyst report noting that Renduchintala’s “departure is not surprising given recent developments of  
26 Intel’s 7nm delay and likely move to a fab-lite and/or fabless business model,” and that “given [Jim]  
27 Keller’s recent departure (the architect [Intel] brought in to fix the mess 2 years ago), the situation is in  
28 total flux. Intel, with or without a move to a [fabless] model over the next several years, is a company in

major upheaval and not at all in control of benefiting from industry transitions, much less its own process and architectural roadmaps. We think that it will take years before things can stabilize for the company. If and when this happens, Intel likely never regains semiconductor excellence and compute supremacy.”

119. On October 1, 2020, the DOE Office of Science provided “broad confirmation” that “the Aurora system”—the DOE’s exascale supercomputer designed around Ponte Vecchio (Intel’s lead 7 nm product)—“will be delayed,” and that Argonne National Laboratory was “currently working with Intel to mitigate the consequences not only to Argonne, but to the Exascale Computing Project and to the nation’s high-performance computing users.”<sup>41</sup> One week later, on October 8, 2020, DOE further revealed that it no longer expected Aurora to be its first exascale supercomputer. Instead, that honor would go to the AMD/TSMC-powered Frontier supercomputer located at Oak Ridge National Laboratory, thus confirming the impact of Intel’s Ponte Vecchio related delays.<sup>42</sup> While declining to provide specifics on Aurora’s status, a senior DOE official confirmed that DOE and Argonne lab officials were “monitoring the situation” and “in discussions with Intel about” the delays and ongoing remediation efforts.<sup>43</sup>

**C. On October 22, 2020, Intel Further Indicates Outsourcing Will Occur as a Result of the 7 nm Delays**

120. On October 22, 2020, following the market’s close, Intel held its Q3 2020 earnings call. During his prepared remarks, Swan provided additional information regarding the Company’s retreat from its existing IDM model towards an expanded semi-fabless model, where all future products would be considered for outsourcing. In this respect, Swan stated that Intel’s “2023 products will deliver on either Intel 7-nanometer or external foundry processes or a combination of both.” In spite of admitting that, at least with respect to its most leading-edge processes, Intel no longer had an IDM advantage, Swan

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<sup>41</sup> See Tiffany Trader, *Aurora’s Troubles Move Frontier into Pole Exascale Position*, HPC Wire (Oct. 1, 2020), <https://www.hpcwire.com/2020/10/01/auroras-troubles-move-frontier-into-pole-exascale-position/>.

<sup>42</sup> See Doug Black, *DOE Under Secretary for Science Dabbar’s Exascale Update: Frontier to Be First, Aurora to Be Monitored*, Inside HPC (Oct. 8, 2020), <https://insidehpc.com/2020/10/doe-under-secretary-for-science-dabbars-exascale-update-frontier-to-be-first-aurora-to-be-monitored/>.

<sup>43</sup> *Id.*

expressed a hope that Intel could “preserve some of the advantages of IDM like schedule, performance and supply as we work with” the foundries.

121. Following Swan’s prepared remarks, Defendant Davis delivered the Company’s financial results. While Intel reported slightly better overall revenue and earnings-per-share results than expected, its gross margins had fallen to 55%, two percentage points below expectations, and its operating margins had fallen to 29%, one percentage point below expectations. Davis also provided Intel’s Q4 2020 forecast; the Company expected its gross margins to fall yet again (to 55%) which would drag its overall 2020 gross margins to 57%.

122. In response to Intel’s announcements, numerous analysts lowered their price targets on the Company as a result of their increasing certainty that at least some portion of Intel’s traditional IDM advantages were now lost for the foreseeable future, as well as the fact that Intel still had no clear solution to its 7 nm woes. For instance, Bernstein lowered its price target to \$40 (from \$45) and, in a note titled “Intel (INTC): 320 Recap – Don’t think it can’t get worse . . .”, recognized that, “[w]hile we thought last quarter’s call was bad, last night’s was potentially even worse as fundamentals are now deteriorating at an alarming pace.” With respect to Intel’s advanced node production, the note “struggle[d] with how the company can have any confidence on achieving 2023 ‘product leadership’ on 7nm (as right now they have no idea what they will be shipping, nor do their customers)” and was “clearly signaling that any solution will consist of some mix of insourced & outsourced volume” while “still . . . investing in [their own] leading edge process. . . . we do not believe any such plan will prove transformational.” The Bernstein analysts added, “Frankly, while CEO Bob Swan suggested 2020 has been the most challenging year in his career, we have to believe that 2021 is going to be worse.” The report concluded by noting, “We got no further information on the current manufacturing issues on last night’s call . . . beyond Intel claiming that their 7nm work was going well, and frankly their credibility on that [7nm] front is infinitesimal.”

123. Similarly, Rosenblatt Securities reiterated its “sell” rating on Intel and lowered its price target from \$45 to \$40, observing that Intel “strategically is now framing 2023 as the year Intel expects product leadership either using their own 7nm, foundry, or both. Things are in flux obviously and 2023 is, well, a truly glacial timeframe in an AI driven world where workload complexity is doubling every



1 few months. Intel has so many moving parts to align, rebuild and/or fix on top of pure innovation that  
2 we struggle to see how they accomplish this feat even with flawless execution given the recent overhaul  
3 of engineering. . . . At the most basic level looking at the shares, the trend here for gross margins is not  
4 good (presumably until 2023).”

5 124. BofA published an analyst report titled “Intel – No easy fix to manufacturing/competitive  
6 headwinds,” in which BofA downgraded Intel to “Underperform” due in part because there was “[n]o  
7 plan/update to fix manufacturing challenges at next-gen 7nm.”

8 125. Also on October 22, 2020, the Portland Business Journal published an article stating that  
9 “[i]n a decision that could profoundly affect Oregon, Intel expects to decide by 2021 whether it will build  
10 its next generation 7-nanometer products in-house or work with a foundry partner. It’s an unthinkable  
11 move for many Intel watchers: The company has always touted its manufacturing as a core differentiator  
12 that’s critical to its product development.”

13 126. As a result of Intel’s disclosures, Intel’s stock price declined **10.57%**, or \$5.70 per share,  
14 from a closing price of \$53.90 per share on October 22, 2020, to a closing price of \$48.20 per share on  
15 October 23, 2020.

16 127. Industry analysts have continued to observe that the prolonged delays in Intel’s 7 nm  
17 process, coupled with the Company’s significant outsourcing plans, contradicted Defendants’ reassuring  
18 statements made during the Class Period, including Swan’s statements on July 23, 2020 that Intel had  
19 supposedly “root caused” the problems and was fixing them. As SemiAccurate recently reported on  
20 January 11, 2021:

21 Best case you could see PR [public relations] quantities of 7nm parts trickle out in the  
22 waning days of 2022 but we put low odds on that at the moment. Bear in mind that 7nm  
23 is a process that Intel was claiming would be out about now (1H/21) as little as 18 months  
24 ago. . . . ***Intel management has repeatedly downplayed crippling problems and has more  
skeletons in the closet than anyone understands. Every time an opportunity presents  
itself to come clean, management does the opposite***, the 7nm “root cause” “disclosure” is  
25 a prime example of that. They don’t know when to stop digging . . . .

26 128. Days later, on January 13, 2021, Intel announced that Swan would be departing the  
27 Company on February 15, 2021. *MarketWatch* noted that Swan “oversaw a tumultuous period for Intel,  
28 as the Company fell behind on its process technology.” That same day, *The Wall Street Journal* wrote

1 that the leadership change was made as Intel “fell further behind rivals in churning out the most advanced  
2 chips.” *The New York Times* wrote that “Intel’s board moved to end Mr. Swan’s tenure as the company  
3 grapples with the fallout from manufacturing problems that have ceded its longtime technology lead to  
4 production services offered by [TSMC] and Samsung Electronics.” Similarly, CNN published, “Under  
5 Swan, the company has struggled, losing market share to competitors in key business segments and  
6 dealing with manufacturing delays.”

## 7 **VI. DEFENDANTS’ MATERIALLY FALSE AND MISLEADING STATEMENTS** 8 **AND OMISSIONS**

9 129. Given the history described above, the market was keenly focused on the status of Intel’s  
10 7 nm process, and in particular the Company’s ability to successfully manufacture the 7 nm process in-  
11 house (as an IDM) according to the stated schedule (unlike the disappointment that was 10 nm). At a  
12 high level, the successful development and timely launch of the 7 nm process node would serve as a  
13 meaningful reacceleration of Intel’s efforts to regain leadership in the industry. It would also mean the  
14 first step in re-attaining the cadence of technology improvement (i.e., 2 to 2.5 years) that Defendants  
15 repeatedly touted during the Class Period. It could also help Intel move beyond the years-long debacle  
16 that the 10 nm node has posed to the Company, leave that difficult portion of its recent history in the past,  
17 and help Intel rebuild its credibility.

18 130. The centrality of the 7 nm node to Intel’s financial future meant that the state of its  
19 progress was the subject of intense public scrutiny and had been for years. In this regard, any hint of  
20 trouble or delay could signal a repeat of the series of drawn-out rolling delays that defined Intel’s 10 nm  
21 saga—but this time without the benefit of a multi-year process node lead to absorb competitive and  
22 economic impacts of such a delay. A failure or extended delay of 7 nm would mean that Intel’s fabs (its  
23 manufacturing capability) had fallen further into unproductiveness and uncompetitiveness. Furthermore,  
24 unlike in the past, Intel’s missteps in developing leading-edge process nodes could not simply be  
25 attributed to the fact it was pioneering new technology, while others merely followed in its path. Rather,  
26 that trailblazer was now TSMC, which had already demonstrated that it could efficiently manufacture  
27 7 nm chips at high volumes, and was now making similar headway into 5 nm process sizes.  
28

131. As described above, prior to the start of the Class Period Intel’s executives emphasized the many “lessons” they had learned going through the painful 10 nm development and yield ramping process, and how by applying those lessons, they knew that Intel’s 7 nm process was “well dialed in” and “making good progress,” and therefore “on track” for a launch in 2021 with Ponte Vecchio, and a “full portfolio” including server CPUs in 2022. Yet, as alleged herein, 7 nm was not on track and, by the start of the Class Period, Defendants knew that 7 nm would be delayed due to development and manufacturing issues. Indeed, by December 12, 2019, Intel had already changed its internal product roadmap to reflect a one-year delay. And as anticipated by this change in its roadmap, on March 31, 2020, Intel missed its hard tapeout deadline for its first 7 nm product, Ponte Vecchio. Nevertheless, throughout all of this, as set forth below, Defendants continued to falsely state to the market that 7 nm was “on track.”<sup>44</sup>

**A. October 24, 2019 – Q3 2019 Earnings Call**

132. False and Misleading Statements. The Class Period begins on October 24, 2019, when Intel hosted a call with analysts to discuss its Q3 2019 results. During his prepared remarks, Defendant Swan emphasized the state of Intel’s 7 nm progress:

As we discussed at the May [2019] investor meeting, we are accelerating the pace of process node introductions and moving back to a 2- to 2.5-year cadence. Our process technology and design engineering teams are working closely to ease process design complexity and balance schedule, performance, power and cost. ***We are on track to launch our first 7-nanometer-based product, a data center-focused discrete GPU, in 2021, 2 years after the launch of 10-nanometer.***

133. During the question-and-answer session, a BMO Capital Markets Equity Research analyst asked Swan about Intel’s plans to accelerate its cadence:

Bob, I wanted to go through the priority and the cadence that you talked about, bringing it back to 2, 2.5 here. Is that -- because my understanding is that they were just simply laws of physics that were causing the cadence to stretch out. So what problems have the engineers and the process folks solved out there? Or is it just limited to the 7-nanometer, and then you would revisit that again?

---

<sup>44</sup> The statements made by Defendants that are emphasized in bold and italics are generally the statements alleged to be false and misleading.

1           134. In response, Swan summarized several reasons for confidence in the 7 nm timeline the  
2 Company had laid out:

3           Yes. It's a good question. Last -- back in our Analyst Day, we tried to go through this in  
4 quite a bit of detail, both, one, kind of *our lessons learned coming out of the challenges*  
5 *we had with 10 and how we're capturing those lessons learned as we think about the*  
6 *next 2 generations. . . .*

7           Second, we -- when we put the design rules in for 7-nanometer, we were less aggressive in  
8 terms of density. Our learning from going from 14 to 10 is -- with the benefit of hindsight,  
9 we were just -- we tried to scale at a 2.7 factor, and that was -- that ended up putting too  
10 much indention or revolutionary nodes into the fab environment to meet those kind of  
11 hurdles. And the learning from that is we just can't hit those kind of really aggressive  
12 targets when, to your point, the dynamics are getting increasingly challenging, so lots of  
13 learnings out of 10.

14           Our transition to 10 that we incorporated into 7, the design rules, there's less complexity.  
15 And for the last couple years, we've been working with EUV. Litho has been the challenge.  
16 We've had EUV that we've been working with for a few years now. And we expect to use  
17 EUV as we scale 7. *And we indicated that our first product will be 2 years from this*  
18 *quarter, so fourth quarter of 2021, our first 7-nanometer product will come out. And*  
19 *our expectation is we'll get back on a 2-year cadence in 7 and beyond. So lots of*  
20 *learnings out of 10-nanometer that we've incorporated. And we said back in May and*  
21 *we reiterated today, we expect to be back to a 2- to 2.5-year cadence going forward, at*  
22 *least for the next few nodes.*

23           135. Later in the call, a UBS Investment Bank analyst raised the issue of outsourcing  
24 production of its advanced node chips:

25           And it sounds like the 7-nanometer GPGPU is still on track for 2021. You did talk about,  
26 for the first time, about 5-nanometer. So can you talk a little bit about how you think of  
27 make versus outsource? And really what I'm after is, is sort of anything sacred? Or if  
28 going to a foundry partner to make CPU or maybe even like a chiplet strategy, if that would  
eliminate a significant piece of your competitive disadvantage, would you consider that?  
Or is that sort of off the table for now?

          136. Swan replied as follows:

          Yes. I mean, first to the comment, yes, the -- *nothing new about process relative to what*  
*we said at Analyst Day, ramp 10, 2-year cadence for 7 and our expectations that the*  
*cadence going forward will be more like 2- to 2.5-year time frame.* So intently focused  
on 10 now and 7 for the product you mentioned in the fourth quarter. So we're investing  
to recapture process leadership going forward.

          At the same time, we're going to be extremely open-minded about how do we ensure that  
we're building the best products, and where we build them is something that we'll always  
evaluate. *I think, as you know with the other foundry players, they've been a source of*  
*our capacities over the years. And our expectation is, to the extent that they can do*

1 *something to support our growth better and/or for peak kind of demands*, we're always  
2 going to look at how do we evaluate the opportunity set that's going to position us best to  
3 meet our customers' demand for the growing diversity of products that we have in our  
4 portfolio.

5 137. Davis added that Intel had begun "adding capacity at 7-nanometer":

6 *We continue to add capacity in 14-nanometer and began adding capacity at 7-nanometer*  
7 *as well. So we're very focused on getting the capacity in place that will allow us to take*  
8 *the word shortage out of our quarterly discussions.*

9 138. Following the Q3 earnings call, Intel's stock traded over \$56.00 per share and securities  
10 analysts were buoyed by Swan's positive 7 nm messaging. For example, on October 24, 2019, Deutsche  
11 Bank analysts rated Intel "Buy" and assigned the stock a price target of \$62.00 per share, stating: "We  
12 applaud the company's aggressive tack towards fixing its manufacturing and accelerating its product  
13 roadmap" and praising Intel's "aggressive manufacturing roadmap (10nm on track in 2H19, 7nm in 4Q  
14 2021) . . . ."

15 139. Also on October 24, 2019, Wells Fargo noted "7nm on Track for 2021" and that "[w]ith  
16 a focus on Intel's emphasis on 7nm being a *fast follower* to 10nm, we will remain focused on the  
17 company's comments / reiteration of targeting 7nm launches in the 2021 timeframe; providing a 2x  
18 improvement in density over 10nm and comparable to competitors at 5nm. Intel's presentation notes that  
19 it is moving back to a 2.0-2.5 year technology cadence; noted that it is on-track for 7nm GPU in 2021."

20 140. Also on October 24, 2019, Bank of America Merrill Lynch published an analyst report  
21 noting that "[Intel] is . . . on track to launch the first 7nm based products in 2021 (two years after 10nm)."

22 141. On October 25, 2019, J.P. Morgan analysts applauded Intel's "Improving Execution,"  
23 noted that "[t]he team . . . remains on track for its first 7nm products in 2021," rated Intel's stock  
24 "Overweight," and increased their price target to \$68.00 per share.

25 142. Reasons Why Defendants' Statements in ¶¶ 132-37 Were Knowingly False and  
26 Misleading: As set forth in ¶¶ 132-37, Defendants made a number of statements representing that Intel's  
27 development of its 7 nm process was on track, including that: (i) Intel was "on track to launch our first  
28 7-nanometer-based product, a data center-focused discrete GPU, in 2021, 2 years after the launch of 10-  
nanometer"; (ii) in the "fourth quarter of 2021, our first 7-nanometer product will come out";  
(iii) Defendants had "nothing new [to explain] about [our manufacturing] process relative to what we

1 said at Analyst Day”; and (iv) that the Company’s “lessons” and “learnings out of 10-nanometer” had  
2 been “incorporated” and “capture[d]” for 7 nm. These statements were materially false and misleading  
3 when made and/or omitted material information because, in truth, by this point in time Intel’s 7 nm  
4 process was already substantially delayed, as alleged in detail above. See ¶¶ 75-79, 103-06.

5 143. As set forth in ¶¶ 132-37, Defendants also made a number of statements that were  
6 materially misleading because they created the untrue impression that Intel was not planning to outsource,  
7 and was in fact not outsourcing, the manufacturing of its leading-edge 7 nm technology to its competitor  
8 foundries, such as TSMC. For instance, when confronted directly with the question of whether, in terms  
9 of “make versus outsource,” “anything [was] sacred” within Intel, or if “going to a foundry partner to  
10 make CPU or maybe even like a chiplet strategy” was “off the table for now,” Swan left analysts with  
11 the erroneous impression that any expanded outsourcing would be consistent with the type Intel was  
12 already doing, i.e., “the other foundry players, they’ve been a source of our capacities over the years,”  
13 and Intel would continue along those lines “to the extent that they can do something to support our growth  
14 better and/or for peak kind of demands.” ¶ 135. Defendant Davis added that Intel had already begun  
15 “adding capacity at 7-nanometer” and was “very focused on getting the capacity in place,” which implied  
16 a strategy that which would rely on internal, rather than outsourced capacity, for the 7 nm product. ¶ 137.

17 144. Similarly, the statement that Intel had “nothing new” to discuss about its efforts to  
18 “recapture [its] process leadership,” was materially misleading because they failed to disclose that, in  
19 fact, Intel was already in the process of outsourcing some 7 nm production—a step that was  
20 unprecedented in Intel’s history and devastating to its IDM business model.

21 145. Likewise, the statements concerning the lessons Intel “captur[ed]” or “incorporated,”  
22 ¶ 134, out of the 10 nm “learnings” or “lessons,” as explained by Defendant Swan on July 23, 2020, were  
23 materially misleading. These statements failed to disclose that one of these “lessons” was that Intel’s  
24 manufacturing capabilities were inadequate, it needed to outsource at least some 7 nm production to a  
25 rival, and was in fact already designing its chips to do so.

26 146. Finally, while Defendant Swan acknowledged that Intel would “evaluate” “other foundry  
27 players” he failed to disclose that at this time the Company had already initiated plans to outsource  
28 production for its leading-edge 7nm products and was in fact already designing its chips to do so.

1           **B.      November 4, 2019 – *Barron's* Publishes an Interview of Defendant Davis**

2           147.   False and Misleading Statements. On November 1, 2019, Davis gave an interview with  
3 *Barron's* which was published on November 4, 2019. This article quoted Davis as saying that “*we’re*  
4 *moving to a two to two and a half year cadence on the next nodes. So we’re pulling in the spending*  
5 *on 7 nanometer, which will start up in the second half of 2021 . . .*”

6           148.   Reasons Why Defendants’ Statements in ¶ 147 Were Knowingly False and Misleading:  
7 As set forth in ¶ 147, Defendant Davis’s statements representing that “7 nanometer . . . will start up in  
8 the second half of 2021” were materially false and misleading when made and/or omitted material  
9 information because, in truth, by this point in time Intel’s 7 nm process was already substantially delayed,  
10 as alleged in detail above. See ¶¶ 75-79, 103-06.

11           **C.      November 4, 2019 – Benchmark’s “Takeaways from CFO Breakfast”**

12           149.   False and Misleading Statements. On November 4, 2019, Benchmark published an  
13 analyst report stating that “[w]e attended a breakfast meeting with George Davis, [Intel’s] CFO, on Friday  
14 [November 1, 2020].” Benchmark summarized Davis’s statements at the breakfast:

15           [Intel] said that . . . capital efficiency will begin to improve at a faster rate at the 7nm node  
16 as EUV is inserted into the manufacturing process. [Intel’s] mindset at this point appears  
17 to be “hit the mark,” meaning that the Company expects to do whatever it takes to meet  
18 product schedule expectations. To that end, *[Intel] remains committed to node transitions*  
19 *on a 2 to 2.5 year cadence.* Interestingly, [Intel] said that it has no interest in being a  
20 Foundry any longer as TSMC’s business model is very different from [Intel’s] and *[Intel]*  
*expects its IDM model to be intact for the foreseeable future. On the flip-side, [Intel]*  
*does not seem very interested in outsourcing capacity needs.*

21           150.   Also on November 4, 2019, Morgan Stanley published an analyst report titled “[Intel]  
22 meeting with CFO reinforces longer-term opportunities,” noting that “[o]n Friday, we attended a small  
23 group meeting with the CFO [i.e., Davis].” Morgan Stanley wrote that “a clear focus on the opportunities  
24 around . . . 7 nm is a step in the right direction, in our view” and, as a result, gave Intel’s stock a price  
25 target of \$65.00 and a rating of “Overweight.”

26           151.   Reasons Why Defendants’ Statements in ¶ 149 Were Knowingly False and Misleading:  
27 As set forth in ¶ 149, Defendant Davis’s statements to the effect that “[Intel] remains committed to node  
28 transitions on a 2 to 2.5 year cadence” were materially false and misleading when made and/or omitted

material information because, in truth, Intel’s 7 nanometer process was already substantially delayed, as alleged in detail above. See ¶¶ 75-79, 103-06.

152. Further, Davis’s statements representing that Intel “expects its IDM model to be intact for the foreseeable future” and that the Company “does not seem very interested in outsourcing capacity needs” were materially false and misleading when made and/or omitted material information because they failed to disclose that, in fact, Intel was already in the process of outsourcing some 7 nm production—a step that was unprecedented in Intel’s history and devastating to its IDM business model.

**D. December 3, 2019 – Credit Suisse Technology, Media and Telecom Conference**

153. False and Misleading Statements. On December 3, 2019, Swan presented at the Credit Suisse Technology, Media and Telecom Conference. During the conference, Swan responded to an inquiry regarding why Intel was so confident in getting back to a 2 to 2.5 year cadence in producing its seven-nanometer chip, despite the challenges and delays the Company faced with its 10-nanometer chip:

[Analyst:] You mentioned earlier your desire to get back on to a two, 2.5 year cadence, as you transition to 7-nanometers. Help the audience to get a better understanding as to why you’re still confident you can make that statement. Given the issues you had at 14 initially, the well-publicized challenges at 10-nanometer, is this solely a function of now having EUV brought into the manufacturing facility or are there other things going on behind the scenes on sort of the design of the chips and the IP blocks that you’re using?

[Swan:] Yes, I mean it’s – maybe start with a function of scar tissue. And scar tissue meaning the challenges that we had and the learnings we got from the 22 nanometer to 14 nanometer transition, the 14 nanometer to 10 nanometer transition. In light of that, how are you learning from the past that builds your confidence in the future.

So, maybe I’ll just start characterizing it that way. We have some scar tissue. The scar tissue really started with Moore’s Law, two times scaling factor every two to 2.5 years. So that’s kind of the simple rule of thumb that’s worked for a very long-time.

\* \* \*

*So, along the way, we -- based on our confidence of past performance, we set a higher and higher bar and it didn’t work effectively. Just took too long. And now, good news is we feel like we’ve got a fairly well dialed in. The bad news is it took too long. . . .*

\* \* \*

*Secondly, we’re not going to try to do 2.4 scaling or 2.7 scaling. As we think about 7-nanometer, we put 2.0 back in line with historical trends.* As we think about 5-nanometer, which would be our competitor’s 3-nanometer, it’s more like 2.0 we’re thinking about. So, we’re not putting as much challenge on the fab and not taking on so much complexity in



design rules, which -- the more there are the more complicated -- the more complicated it is. *So we're capturing these learnings from the past and are applying them going forward.*

*The third thing, to your point is, with 7-nanometer, one of the benefits of, I should say, of 10-nanometer taking long is we've been playing with EUV for a while. So, this is a new generation of technology. We've been playing with it for a while. While 10-nanometer has took long, our teams including our tool provider had lots of time to work through the inherent challenges of bringing the new technology and list them online.*

*So, on the combination of learnings from the past, capturing those learnings, how do we think about those going forward, applying them and then tracking along the way. So 7-nanometers we didn't start it yesterday. We started several years ago and we monitor performance on density, on functionality and based on kind of where we are today, we feel pretty good about getting to a two, 2.5 year cadence and launching our first 7-nanometer product in the fourth quarter of 2021.*

154. Reasons Why Defendants' Statements in ¶ 153 Were Knowingly False and Misleading:

As set forth in ¶ 153, Defendant Swan made a number of statements representing that Intel's development of its 7 nanometer process was on track, including that: (i) Intel had its transition to its next (7 nm) process node "fairly well dialed in"; (ii) that "we're capturing these learnings from the past [i.e., Intel's experience with '10-nanometer taking long'] and are applying them going forward" (i.e., to 7 nm); (iii) that Intel was on track to resuming "a two, 2.5 year cadence and launching our first 7-nanometer product in the fourth quarter of 2021"; and (iv) that "[w]e started several years ago and we monitor performance on density, on functionality and based on kind of where we are today, we feel pretty good about getting to a two, 2.5 year cadence and launching our first 7-nanometer product in the fourth quarter of 2021."

155. These statements were materially false and misleading when made and/or omitted material information because, in truth, Intel's 7 nanometer process was already substantially delayed, as alleged in detail above. *See* ¶¶ 75-79, 103-06. Among other things, on December 12, 2019, SemiAccurate reported that Intel's "roadmaps" for its "7nm server CPUs . . . unquestionably" said that they would first be available in "late 2023." *See* ¶ 77.

**E. December 10, 2019 – UBS Global Technology, Media and Telecommunications Conference**

156. False and Misleading Statements. On December 10, 2019, Renduchintala represented Intel during a presentation at the UBS Global Technology, Media and Telecommunications Conference.

1 During the conference, in response to a question from an analyst about “what you’ve learned” from Intel’s  
2 10nm experience, Renduchintala explained that the Company had “learned a number of really, really  
3 crucial lessons” from the challenges it faced in the development and production of its 10-nanometer  
4 technology:

5 [Analyst:] I think there’s a lot of common elements between 10 nanometer and between  
6 7 nanometer, given the issues that you’ve had on 10, which have been quite public, can  
7 you talk about what you’ve learned that might give us more confidence on 7, this is a  
8 question that I get time and time again, I spend hours and hours talking about this every  
9 week. So, can you just hold out (inaudible) there a little bit?

10 \* \* \*

11 [Renduchintala:] Sure. But first of all, as somebody who regards themselves of the  
12 technologies first and foremost, you go through your career very much understanding that,  
13 your most seminal learnings come from the programs or the activities you were part of that  
14 didn’t go according to plan. ***And with 10 nanometers, I think the company has learned  
15 a number of really, really crucial lessons that I think sets us up to be a much, much more  
16 mature decision-making organization going forward.***

17 ***I would say, on 10, we learned four key lessons. The first is really to balance the pursuit  
18 of scaling and cost together with schedule predictability power and performance.*** And  
19 Intel was very focused on continuing to achieve a cost per transistor curve, that complied  
20 with the Moore’s Law cadence of every 2 years. And I think in doing that, in the last stages  
21 of immersion lithography, we had an extremely large leap to stay on that curve, we had to  
22 achieve a 2.7 at scaling factor from 14 to 10 to be on that curve. And when you go to that  
23 level of scaling, it requires a tremendous amount of fundamental innovation. And I think  
24 the real lesson we learned is that, the amount of innovation that we put together in order to  
25 make that transistor scaling factor while we had confidence in each of the elements  
26 individually, when we brought them together, the confluence of all those technology  
27 innovations gave us a lot of permutation and combination interaction effects that we had  
28 to spend quite a bit of time untangling.

***So going forward on 7, we’ve taken a much more pragmatic approach of basically  
making sure the scaling risk we take doesn’t perturbate our ability to deliver to schedule  
and to power and performance.*** So as we’ve said in the past, we’ve moved more to a  
scaling factor around 2x between 10 and 7. ***The other thing that we learned and this was  
very much a lesson we learned on 14 is to continue to harvest intra-node product  
optimizations or intra-node process optimizations. . . .***

***The third [lesson learned] is to maintain a mix of nodes, going forward as well not out  
of one node into another node in full gusto, but essentially take a much more gradual  
and measured migration between nodes, because not every part of technology that we  
deliver in an SoC benefits proportionately from logic scaling.*** So, for concerns of time to  
market, power and performance and margin maintaining a mix of nodes going forward in  
a heterogeneous product construction approach is really important.

1 *And the final lesson, probably one of the most important lessons is to make it easy and*  
2 *fast for our design teams to be able to migrate through intra-node transitions.* For us  
3 one of the key things we've really done is to make sure that as we've delivered process  
4 goodness, we've also made that much easier for our design teams to pick up and run with  
5 so that we can get much greater velocity in our product cadence. *So all of those have been*  
6 *integrated into our approach on 7. And I think we're making good progress on 7 as a*  
7 *result of that. And as we've announced previously, we'll see our first 7 nanometer*  
8 *product shipping in 2021 with a full portfolio in 2022.*

9 \* \* \*

10 [Analyst:] Got it. Great, thank you. Just on -- just keeping on that theme, why did you  
11 choose a general purpose GPU to be the lead vehicle for 7 nanometer. And maybe if you  
12 can remind us when you're going to have a 7 nanometer CPU?

13 [Renduchintala:] . . . [T]he GPGPU, or GPU in general benefits from the scaling and  
14 performance and power advantage that come with the transition from 10 to 7 as  
15 significantly as for example as CPU. And thirdly, [a] *GPGPU by nature of its architecture*  
16 *and redundancy in the architecture makes it a lot more amenable to being a good ramp*  
17 *vehicle in the early phases of a new node where defect density is still being pushed down*  
18 *to its absolute minimum. But there won't be a large gap between the launch of our first*  
19 *product in 7 and the rest of our portfolio. So you can expect a full portfolio of products*  
20 *across our entire product portfolio within a year of that first product launch.*

21 157. Renduchintala also assured investors that Intel was not in the process of making any  
22 significant changes to its IDM model, again in response to an analyst's questions on the subject:

23 [Analyst:] . . . I know that TSMC already is a supplier of yours today, but can you talk  
24 about the pluses and minuses with engaging more deeply with a foundry partner. And can  
25 you talk about, would you ever consider outsourcing CPU why, why not. I know Bob  
26 certainly sounds a lot more open to outsourcing, but can you just talk about that. Thank  
27 you.

28 [Renduchintala:] Yeah, well, first of all, I think we regard companies like TSMC and  
Samsung as strategic partners. Intel's had a long history, over two decades of history of  
working with the foundry ecosystem. And in fact, something like 20% to 25% of the wafer  
volume that we source comes from outside of the Company and *we don't see that changing*  
*in any major fashion going forward.*

And quite frankly there is a lot to learn from engaging with the fabless ecosystem. I mean  
it's an incredibly insular attitude to assume that everything that we do inside Intel is perfect  
by engaging with the external foundries and the third party ecosystems that fuel that  
foundry ecosystem. We learn a tremendous amount that makes us a better IDM.

But that said, *we still believe that there is tremendous value in the IDM approach we have*  
*going forward.* And if you look at the assets that Intel brings to bear, we have process  
technology, we have advanced packaging technology; we have memory technology; we  
have interconnect technology, *we also have an incredibly important franchises at CPU,*  
*which is a cornerstone IP;* we're building a portfolio of what we call xPU architectures  
like the GPU, the FPGA, the neural network processes. And we're integrating that with

1 really strong focus on both security and harmonizing software. *And if you integrate all of*  
2 *that together, you get an incredibly potent innovation environment, that's very difficult*  
3 *to replicate in a fabless foundry partnership. So while we think, there is great value*  
4 *engaging with and learning from the external foundry ecosystem, we still think that there*  
5 *is tremendous generate -- a value we can generate by continuing to be an IDM.* So we  
6 play those positions intelligently and pragmatically to deliver the best portfolio we can for  
7 our customers.

8 158. The market reacted positively to Renduchintala's statements. For example, that same day,  
9 UBS analysts published a report with "[c]ommentary on . . . [d]e-risking 7nm" reporting that "[Intel]  
10 noted that it had learned the lessons from 10nm challenges i.e. having taken on an extremely large leap  
11 towards a 2.7x shrink factor in 10nm. [Intel] is now taking a more pragmatic approach to 7nm - balancing  
12 scaling and cost with predictability and schedule and opting for a more conservative ~2x shrink factor."  
13 UBS further reported: "GPGPU as lead product for 7nm: [Intel] . . . sees the GPGPU as an ideal  
14 architecture to ramp up process yields given its much tighter margin requirements. [Intel] indicated that  
15 there would be no large gap between GPGPU (we think H2;21) and the rest of the 7nm portfolio w/-  
16 entire product portfolio on 7nm within a year of GPGPU launch." Regarding Intel's "[c]ommentary on  
17 [o]utsourcing [manufacturing]," UBS noted that "[Intel] noted that while it is engaging with foundry  
18 ecosystem and learning a lot, it still sees tremendous value in the IDM approach, meaning, while [Intel]  
19 regards TSMC and Samsung as strategic partners (20-25% of wafer volume comes from outside [Intel]),  
20 it does not think it will change meaningfully in the near term." UBS gave Intel's stock a "12-month  
21 rating" of "Buy" and a "12m price target" of \$60.00.

22 159. Reasons Why Defendants' Statements in ¶¶ 156-57 Were Knowingly False and  
23 Misleading: As set forth in ¶¶ 156-57, Defendant Renduchintala made a number of statements  
24 representing that Intel's development of its 7 nm process was on track, including that that "we'll see our  
25 first 7 nanometer product shipping in 2021 with a full portfolio in 2022." These statements were  
26 materially false and misleading when made and/or omitted material information because, in truth, Intel's  
27 7 nm process was already substantially delayed, as alleged in detail above. See ¶¶ 75-79, 103-06. Indeed,  
28 just two days later, on December 12, 2019, SemiAccurate reported that Intel's "roadmaps" for its "7nm  
server CPUs . . . unquestionably" said that they would first be available in "late 2023." See ¶ 77.

160. As set forth in ¶ 156, Renduchintala also made a number of misleading statements to the  
effect that "the company has learned a number of really, really crucial lessons" including "four key

1 lessons” on “10 [nm],” including “to balance the pursuit of scaling and cost together with schedule  
2 predictability power and performance” and that as a result “on 7 [nm], [we have] taken a much more  
3 pragmatic approach of basically making sure the scaling risk we take doesn’t perturbate our ability to  
4 deliver to schedule and to power and performance.” Renduchintala also claimed that “we’re making  
5 good progress on 7 [nm] as a result of” those “lessons.” These statements were materially false and  
6 misleading, however, because Intel’s “ability to deliver to schedule” was already “perturbate[d]” because,  
7 among other things, Intel’s roadmap for its 7 nm server CPU chips had been extended well into late 2023.

8 161. Furthermore, Renduchintala’s statements that “we learned four key lessons” from 10-  
9 nanometer, that “all of those [lessons] have been integrated into our approach on 7,” and “I think we’re  
10 making good progress as a result of that” were materially misleading because Renduchintala failed to  
11 mention, as Defendant Swan acknowledged on July 23, 2020, that the Company had in place  
12 “contingency plans” to externally manufacture some of its leading-edge 7-nm products. In other words,  
13 one of the “lessons” learned from 10 nm was that Intel’s manufacturing capabilities were inadequate, and  
14 it needed to outsource at least some 7 nm product to a rival. This omission also allowed Defendants to  
15 conceal that the “tremendous value” of Intel’s IDM business model was at risk, because if Intel relied,  
16 even in part, on external foundries for its leading-edge products, this would greatly call into question the  
17 Company’s business model going forward.

18 162. Finally, as set forth in ¶ 157, Renduchintala also made a number of statements that were  
19 materially misleading because they created the untrue impression that Intel was not planning to outsource,  
20 and was in fact not, outsourcing, the manufacturing of its leading-edge 7 nm technology to its competitor  
21 foundries. Renduchintala’s statements that “we still believe that there is tremendous value in the IDM  
22 approach we have” and “there is tremendous . . . value we can generate by continuing to be an IDM,”  
23 were misleading because they failed to disclose that, at that time, Intel was already in the process of  
24 outsourcing some 7 nm production—a step that was unprecedented in Intel’s history and devastating to  
25 its IDM business model. *See* ¶¶ 78, 103-06, 120.

## 26 **F. January 23, 2020 – Q4 2019 Earnings Call**

27 163. False and Misleading Statements. After the market close on January 23, 2020, Intel hosted  
28 an earnings conference call with analysts to discuss its Q4 2019 and FY 2019 results. Swan once again

emphasized that “[o]ur 7-nanometer process remains on track to deliver our lead 7-nanometer product, Ponte Vecchio, at the end of 2021, with CPU products following shortly after in 2022.”

164. The market reacted positively to Swan’s statements. The next day after the Q4 2020 earnings call, on January 24, 2020, Intel’s stock traded above \$69.00 per share. Securities analysts also reacted positively. For example, on January 23, 2020, UBS analysts reported that “there was no wavering on 10/7nm timelines” and raised its price target from \$60.00 to \$75.00 per share.

165. Similarly, on January 24, 2020, J.P. Morgan analysts wrote that “the [Intel] team remains on track for its first 7nm products (Ponte Vecchio) in 2021,” rated the stock “Overweight,” and raised its price target from \$68.00 to \$80.00 per share.

166. Reasons Why Defendants’ Statements in ¶ 163 Were Knowingly False and Misleading: As set forth in ¶ 163, Defendant Swan made a number of statements representing that Intel’s development of its 7 nm process was on track, including that: (i) “[Intel’s] process technology execution continues to improve”; and (ii) its “7-nanometer process remains on track to deliver our lead 7-nanometer product, Ponte Vecchio, at the end of 2021, with CPU products following shortly after in 2022.” These statements were materially false and misleading when made and/or omitted material information because, in truth, Intel’s 7 nanometer process was already substantially delayed, as alleged in detail above. See ¶¶ 75-79, 103-06. Among other things, by no later than December 2019, Intel’s roadmaps for its 7 nm server had been pushed back by a year. See ¶ 77.

**G. January 24, 2020 – 2019 Form 10-K**

167. False and Misleading Statements. On January 24, 2020, Intel filed with the SEC its annual report on Form 10-K for the fourth quarter and full fiscal year 2019. The Form 10-K was signed by Defendants Swan and Davis. The Form 10-K stated in relevant part:

*We are accelerating the pace of process node introductions and moving back to a 2- to 2.5-year cadence. We are on track to deliver our first 7nm-based product, a discrete GPU, at the end of 2021.*

\* \* \*

*We are an IDM. Unlike many other semiconductor companies, we primarily design and manufacture our products in our own manufacturing facilities, and we see our in-house manufacturing as an important advantage.* We continue to develop new generations of manufacturing process technology as we seek to realize the benefits from Moore’s Law. Realizing Moore’s Law results in economic benefits as we are able to either reduce a chip’s

1 cost as we shrink its size, or increase functionality and performance of a chip while  
2 maintaining the same cost with higher density. This makes possible the innovation of new  
3 products with higher performance while balancing power efficiency, cost, and size to meet  
4 customers' needs. ***Our ability to optimize and apply our manufacturing expertise to  
5 deliver more advanced, differentiated products is foundational to our current and future  
6 success.***

7 We improved our 10nm factory production, yield, and volume during 2019, and launched  
8 10th-generation Intel® Core™ processors, our first 10nm volume product, and Intel®  
9 Agilex™, our first 10nm FPGA. We expect to deliver initial production shipments of our  
10 first 10nm-based Intel® Xeon® Scalable product, Ice Lake, in the latter part of 2020.

11 ***We are on track to deliver our first 7nm-based product, a data center-focused discrete  
12 GPU, at the end of 2021. We are approaching next-generation process nodes with a  
13 focus on striking an optimal balance between schedule, performance, power, and cost  
14 and will continue to drive intra-node advancement.***

15 Our technology and innovation pipeline is as full and as strong as it's ever been. By  
16 embracing our ecosystems and delivering new capability on a predictable cadence, we will  
17 continue to drive Moore's Law forward and create compelling products for our customers.

18 168. Further assuring investors of the veracity of these statements, the 2019 Form 10-K  
19 included a certification signed by Swan and Davis, as required by the Sarbanes-Oxley Act of 2002  
20 ("SOX"), representing that ***"this report does not contain any untrue statement of a material fact or omit  
21 to state a material fact necessary to make the statements made, in light of the circumstances under  
22 which such statements were made, not misleading with respect to the period covered by this report."***

23 169. Reasons Why Defendants' Statements in ¶ 167 Were Knowingly False and Misleading:  
24 As set forth in ¶ 167, Intel's 2019 Form 10-K made a number of statements representing that the  
25 Company's development of its 7 nm process was on track, including that: (i) "[w]e are accelerating the  
26 pace of process node introductions and moving back to a 2- to 2.5-year cadence"; and (ii) "[w]e are on  
27 track to deliver our first 7nm-based product, a discrete GPU, at the end of 2021." These statements were  
28 materially false and misleading when made and/or omitted material information because, in truth, Intel's  
7 nm process was already substantially delayed, as alleged in detail above. *See* ¶¶ 75-79, 103-06. Among  
other things, by no later than December 2019, Intel's roadmaps for its 7 nm server had been pushed back  
by a year. *See* ¶ 77.

170. As set forth in ¶ 167, Intel's 2019 Form 10-K also made a number of statements that were  
materially misleading because they created the untrue impression that Intel was not planning to outsource,  
and was in fact not, outsourcing, the manufacturing of its leading-edge 7 nanometer technology to its

competitor foundries. Specifically, the 2019 Form 10-K stated that (i) “[w]e are an IDM”; (ii) “[u]nlike many other semiconductor companies, we primarily design and manufacture our products in our own manufacturing facilities, and we see our in-house manufacturing as an important advantage”; and (iii) “[o]ur ability to optimize and apply our manufacturing expertise to deliver more advanced, differentiated products is foundational to our current and future success.” These statements were materially false and misleading because they failed to disclose that, in fact, Intel was already in the process of outsourcing some 7 nm production to a rival—a step that was unprecedented in Intel’s history and devastating to its IDM business model.

171. In addition, the SOX certification signed by Swan and Davis, *see* ¶ 168, was materially false and misleading because the 2019 Form 10-K did contain material misrepresentations and omissions of fact as alleged herein.

**H. March 2, 2020 – Morgan Stanley Technology, Media & Telecom Conference**

172. False and Misleading Statements. On March 2, 2020, Davis represented Intel during a presentation at the Morgan Stanley Technology, Media & Telecom Conference. During the conference, an analyst asked Davis about Intel’s progress on its 10-nanometer and 7-nanometer process technology:

[Analyst:] . . . So can you talk about the progress of 10-nanometer and 7-nanometer and your confidence level going forward there?

\* \* \*

[Davis:] . . . But so I feel like we’re in the 10-nanometer node. It’s important that we’re continuing to see yield improvements ratably over the time period. But as we said back in our Analyst Day in May of ‘19, look this isn’t going to be the best node that Intel has ever had. It’s going to be less productive than 14, less productive than 22, but *we’re excited about the improvements that we’re seeing and we expect to start the 7-nanometer period . . . with a much better profile of performance over that starting at the end of ‘21.*

\* \* \*

[Analyst:] . . . But it seems like the biggest thing for me is, from a planning process, it seems like Intel’s on a pretty firm foundation. I mean, you didn’t when 10 was delayed, it obviously means you don’t have your best foot forward product wise either. Seems right now say very at least the next couple of years there is a very clear stepping stone roadmap for where we’re going to go?

[Davis:] *Yeah, I think we feel very good about where the road map is going. . . . we feel like we’re starting to see the acceleration on the process side that we have been talking*



1 *about to get back to parity in the 7-nanometer generation and regain leadership in the*  
2 *front down there.*

3 173. The market reacted positively to Davis's statements. For example, BofA analysts reported  
4 that "CFO George Davis participated in a fireside chat at a sell-side conference this morning," and wrote  
5 that Intel was "well on its way to working through past issues" and that "management already has its  
6 sight set on transitioning to what it expects to be a more productive/performant 7nm node by the end of  
7 2021," rated Intel's stock "BUY" and gave it a "Price Objective" of \$75.00. The same day, Wells Fargo  
8 analysts reported that "Mr. Davis . . . noted that Intel is focused on . . . achieving parity at 7nm node and  
9 then regaining leadership in subsequent 5nm . . . focus on fast move to 7nm process node into 2021 (led  
10 with data center GPUs; Ponte Vecchio) – emphasizing confidence in where Intel is going on their  
11 roadmap," and assigned Intel's stock a price target of \$70. The next day, Morgan Stanley analysts wrote  
12 that "Intel (CFO George Davis) continues to sound upbeat about its prospects and long term strategy"  
13 and "[t]he company . . . repeated its commitment to ship 7 nm product in late 2021."

14 174. Reasons Why Defendants' Statements in ¶ 172 Were Knowingly False and Misleading:  
15 As set forth in ¶ 172, Defendant Davis's statements that "we're excited about the improvements that  
16 we're seeing and we expect to start the 7-nanometer period . . . with a much better profile of performance  
17 over that starting at the end of '21" and that "we feel very good about where the road map is going. . . .  
18 we feel like we're starting to see the acceleration on the process side that we have been talking about to  
19 get back to parity in the 7-nanometer generation and regain leadership in the front down there" were  
20 materially false and misleading when made and/or omitted material information because the 7 nm process  
21 was actually substantially delayed, as alleged in detail above. *See* ¶¶ 75-79, 103-06. Among other things,  
22 by no later than December 2019, Intel's roadmaps for its 7 nm server had been pushed back by a year.  
23 *See* ¶ 77.

24 **I. April 23, 2020 – Q1 2020 Earnings Call**

25 175. False and Misleading Statements. On April 23, 2020, Intel held its first quarter 2020  
26 earnings call. During their prepared remarks, neither Swan nor Davis affirmatively raised the topic of  
27  
28

1 the 7 nm process. However, during the question-and-answer session, a Crédit Suisse analyst asked the  
2 following question:

3 I'm just wondering if you could give us a little bit more detail on the gross margin decline  
4 heading into the calendar second quarter. George, you kind of broke it up into 3 different  
5 categories . I'd be interested on magnitude of [10 nm] Tiger Lake versus just lower  
6 volumes and then other 10-nanometer parts. And I guess, more importantly, how do we  
7 think about kind of normalized sort of gross margins as you get past some of the start-up  
8 costs for a faster 10-nanometer ramp?

9 176. Swan responded, in part, by stating that "we plan to get back on a 2- to 2.5 year cadence"  
10 and "we're investing in 7-nanometer that we anticipate having in the fourth quarter of 2021":

11 On the second part of your question, I'd go back to the commentary that George provided  
12 back at our Analyst Day in the spring, which is, obviously, when we transition from a  
13 mature node to a new node, margins tend to come down. *We indicated that we plan to get  
14 back on a 2- to 2.5-year cadence, which means in 2021, we'll be ramping 10-nanometer  
15 even more while we're investing in 7-nanometer that we anticipate having in the fourth  
16 quarter of 2021.* So those dynamics of -- from a mature node to a new node, impacts the  
17 gross margins of the business, but we feel like it's -- *we're well on track from the plans  
18 we laid out* and feel pretty good about a dynamite first quarter and an outlook for the second  
19 quarter in line or better than what we expected.

20 177. Analysts responded positively to Swan's statements. For example, on April 23, 2020,  
21 Crédit Suisse analysts wrote that "we see [Intel]'s accelerating/improving roadmap to 10nm/7nm  
22 products . . . as compelling" and reiterated its target price of \$75.00 and its "Overweight" rating for the  
23 stock.

24 178. On April 24, 2020, J.P. Morgan analysts wrote that "the [Intel] team remains on track for  
25 its first 7nm products in 2021" and concluded that the "team is executing well on its  
26 product/manufacturing roadmaps that positions the team well . . . ." Accordingly, J.P. Morgan gave  
27 Intel's stock a price target of \$80.00 and rated it "Overweight."

28 179. Also on April 24, 2020, analysts at UBS wrote that "[b]ottom line, we remain bullish here  
as . . . the manufacturing narrative is about to gain significant momentum" and "the main fulcrum on the  
investment case remains [Intel's] progress in catching up to TSMC (and, ergo, AMD) on manufacturing  
and we would argue that the read through was, if anything, better as 10nm costs are clearly coming down  
(though always limited) and 7nm remains totally on track." UBS gave Intel's stock a price target of  
\$70.00 and rated it "Buy."

180. Reasons Why Defendants' Statements in ¶ 176 Were Knowingly False and Misleading:

As set forth in ¶ 176, Defendant Swan made a number of statements representing that Intel's development of its 7 nanometer process was on track, including that: (i) Intel would resume its "2- to 2.5-year cadence" of process node transitions; (ii) Intel's first 7 nm chips (Ponte Vecchio) would begin arriving "in the fourth quarter of 2021"; and (iii) "we're well on track from the plans we laid out." These statements were materially false and misleading when made and/or omitted material information because in truth, Intel's 7 nanometer process was already substantially delayed, as alleged in detail above.

181. Indeed, as alleged above, Intel's product roadmaps for its 7 nm process had already been pushed out by a year. Further, Swan's statements failed to disclose that its key first 7 nm chip, the Ponte Vecchio GPU, had already missed a crucial tapeout deadline that rendered impossible internal production of the chip in accordance with the timeframes required to meet the Project Aurora timeline of 2021. ¶¶ 75-79, 84-87, 103-06.

182. Further, as Renduchintala explained on December 10, 2019, Intel had chosen Ponte Vecchio, a GPGPU, to be Intel's "lead vehicle for 7 nanometer" instead of a CPU because a "GPGPU by nature of its architecture and redundancy in the architecture makes it a lot more amendable to being a good ramp vehicle in the early phases of a new node." In short, the fact that Ponte Vecchio had still not yet taped out by the end of March meant not only that Ponte Vecchio, but Intel's entire 7 nm process node effort (including subsequent 7 nm server CPUs) was significantly off track and behind schedule.

**J. June 11, 2020 – Jim Keller Departs**

183. False and Misleading Statements & Partial Corrective Disclosure. On June 11, 2020, Intel announced the abrupt resignation of Keller, effective immediately. Intel also revealed significant leadership changes within TSCG—the group responsible for engineering and manufacturing Intel's semiconductor chips, including its 7 nm process. In the press release announcing the Keller departure, Intel stated the following:

Today, Intel announced that Jim Keller has resigned effective June 11, 2020, *due to personal reasons*. Intel appreciates Mr. Keller's work over the past two years helping them continue advancing Intel's product leadership and they wish him and his family all the best for the future. Intel is pleased to announce, however, that Mr. Keller has agreed to serve as a consultant for six months to assist with the transition.

184. Despite Keller's departure, Intel reassured analysts and investors that its chip engineering and manufacturing group remained strong and that development of the 7 nm chip was on schedule. Specifically, the same day that Intel announced Keller's resignation, June 11, 2020, Swan and Davis met with analysts from Deutsche Bank and discussed, among other things, the Company's progress on its 7 nm transition. Deutsche Bank reported that Defendants Swan and Davis stated that they were "[l]ooking forward to 7nm, [Intel]'s time-line remains unchanged with a late 2021 launch."

185. Reasons Why Defendants' Statements in ¶¶ 183-84 Were Knowingly False and Misleading: As set forth in ¶ 184, Defendants' statement representing that Intel's development of its 7 nm process was on track, including specifically that "[Intel]'s time-line remains unchanged with a late 2021 launch" for 7 nm, was materially false and misleading when made and/or omitted material information because, in truth, Intel's 7 nm process was already substantially delayed. As alleged in detail above: (1) since at least December 2019, Intel's internal roadmaps for its 7 nm server CPU products had been pushed out by a year, ¶ 77; (2) Intel's key first 7 nm chip, the Ponte Vecchio GPU, had already missed a crucial hard tapeout deadline that would render impossible internal production of the chip in accordance with the deadlines required to meet the Project Aurora timeline, ¶¶ 84-87; (3) a set of leaked slides from May 2020 further confirmed that Intel's "Next Gen" 7 nm server CPU would arrive only later in "2023"—not in 2022, as the Company had publicly stated, ¶¶ 90-92; and (4) Intel's manufacturing capabilities were so deficient that it had already begun steps to outsource production of its first 7 nm chip to a rival, ¶¶ 75-79, 103-06, 120.

186. Moreover, it was materially false and misleading to attribute Keller's departure solely to "personal reasons." ¶ 183. Defendants' statements regarding Keller's departure omitted to disclose that, as reported by FE 1, Keller's abrupt departure from Intel was driven by his disagreements with Swan and Renduchintala concerning their refusal to address the known problems with the development of the 7 nm process. See ¶¶ 93-94.

**K. June 25, 2020 – Intel Spokesperson Emails *Consumer Electronics Daily***

187. False and Misleading Statements. On June 25, 2020, *Consumer Electronics Daily* published an article stating that "[a]n Intel spokesperson emailed Wednesday [i.e., June 24, 2020] that *its 7-nanometer process 'remains on track' with first products due by the end of 2021.*"

188. Reasons Why Defendants’ Statement in ¶ 187 Was Knowingly False and Misleading: As set forth in ¶ 187, Intel’s statement to *Consumer Electronics Daily* representing that “[Intel’s] 7-nanometer process ‘remains on track’ with first products due by the end of 2021” was materially false and misleading when made and/or omitted material information because in truth, Intel’s 7 nanometer process was already substantially delayed. As alleged in detail above, (1) since at least December 2019, Intel’s internal roadmaps for its 7 nm products had been pushed out by a year, ¶ 77; (2) Intel’s key first 7 nm chip, the Ponte Vecchio GPU, had already missed a crucial hard tapeout deadline that would render impossible internal production of the chip in accordance with the deadlines required to meet the Project Aurora timeline, ¶¶ 84-87; (3) a set of leaked slides from May 2020 confirmed that Intel’s “Next Gen” 7 nm server CPU would arrive in the second half of “2023”—not in 2022, as the Company had publicly stated, ¶¶ 90-92; and (4) Intel’s manufacturing capabilities were so deficient that it had already begun steps to outsource production of its 7 nm chip to a rival, ¶¶ 103-06. Indeed, just weeks after making this statement, Intel admitted that, in fact, its 7 nm process was delayed by a full year. *See* ¶ 101.

## VII. ADDITIONAL SCIENTER ALLEGATIONS

189. At all relevant times, the Individual Defendants acted with scienter in making materially false and misleading statements during the Class Period. Each of the Individual Defendants had actual knowledge that the statements made by him were materially false and misleading, or acted with deliberately reckless disregard for the truth or falsity of those statements.<sup>45</sup> Each of the Individual Defendants’ intent to deceive and deliberate reckless disregard for the truth is demonstrated by substantial direct and circumstantial evidence supporting a strong inference of scienter. Many of the facts relevant to scienter are set forth above, including that Intel’s own internal product roadmaps and missed hard tapeout deadline contradicted Defendants’ public statements. Certain additional facts supporting a strong inference of scienter are noted below.

### A. Defendants Claimed to “Monitor . . . Progress” on 7 nm “Closely”

190. Before and during the Class Period, Defendants repeatedly told investors that they were closely monitoring Intel’s progress on its 7 nm process. For example, during the July 26, 2018 Q2 2018

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<sup>45</sup> The cumulative knowledge of all members of the Company’s management team, including the Individual Defendants, is properly imputed to Intel.

1 earnings call, Defendant Renduchintala stated that Intel was “focusing on being much more precise in  
2 our ability to launch,” and that “we monitor progress on 7 [nm] just as closely as we are on 10 [nm], I  
3 feel those lessons are being well absorbed into our progress.”

4 191. Likewise, on December 3, 2019, Swan stated that “we didn’t start it [7 nm] yesterday. We  
5 started several years ago and we monitor performance on density, on functionality and based on kind of  
6 where we are today, we feel pretty good about getting to a two, 2.5 year cadence and launching our first  
7 7-nanometer product in the fourth quarter of 2021.”

8 192. Defendants’ knowledge of, or reckless disregard for, the fact that Intel’s 7 nm product and  
9 process was not “on track” is supported by their repeated claims to continuously and closely monitor the  
10 progress of the Company’s 7 nm process.

11 **B. Defendants Attributed Intel’s “Good Progress on 7 [nm]” to the “Really,**  
12 **Really Crucial Lessons” They Had Learned from 10 nm**

13 193. Before and during the Class Period, Defendants repeatedly told investors that Intel’s  
14 “good progress” on 7 nm was the result of “lessons” they had learned from the Company’s 10 nm process.  
15 For example, on May 8, 2019, Renduchintala stated that “7-nanometers will . . . incorporate all the  
16 lessons that . . . we’ve learned in 14 and 10” and “[w]e’ve learned from our 10-nanometer experiences . . .  
17 and we’ve institutionalized and driven those [lessons] into our definition of 7-nanometers, and we’re  
18 executing at full pace per the original schedule that we set out 2 years ago on that 7-nanometer road map.”

19 194. Similarly, on July 26, 2018, an analyst asked Renduchintala “what you’ve learned on 10,  
20 how you’re applying it to 7 and . . . how it’s going.” In response, Renduchintala stated that “key  
21 learnings” from its 10 nm experience were being applied to its 7 nm development and that “those lessons  
22 are being well absorbed into our progress.”

23 195. Swan also raised these “lessons” during the October 24, 2019 earnings conference call,  
24 when he mentioned “our lessons learned coming out of the challenges we had with 10 and how we’re  
25 capturing those lessons learned as we think about the next 2 generations,” and specifically referred to  
26 “design rules . . . for 7-nanometer” that “were less aggressive in terms of density” and contained “less  
27 complexity,” as well as the incorporation of EUV lithography technology at 7 nm that would allow Intel  
28 “to be back to a 2- to 2.5-year cadence going forward, at least for the next few nodes.”

1           196. On December 10, 2019, Renduchintala told investors at the UBS Global TMT Conference  
2 that “with 10 nanometers, I think the company has learned a number of really, really crucial lessons that  
3 I think sets us up to be a much, much more mature decision-making organization going forward.”  
4 Renduchintala elaborated that “all of those [lessons] have been integrated into our approach on 7 [nm].  
5 And I think we’re making good progress on 7 [nm] as a result of that. And as we’ve announced  
6 previously, we’ll see our first 7 nanometer product shipping in 2021 with a full portfolio in 2022.”

7           197. Defendants’ knowledge of, or reckless disregard for, the fact that Intel’s 7 nm product and  
8 process was not “on track” is supported by their repeated claims that the basis for their “good progress”  
9 on 7 nm was the “really, really crucial lessons” they had “learned” from the Company’s 10 nm process.

10           **C. Defendants Knew of Facts Critical to Intel’s Core Operations**

11           198. The Individual Defendants were Intel’s CEO, CFO, and Chief Engineering Officer and  
12 were responsible for, and remained well-informed about, issues critical to the Company’s success. For  
13 Intel, few if any issues were more critical to its success than its ability to progress to more advanced  
14 microprocessor fabrication process nodes in a timely manner and to use those nodes to produce its chips  
15 in a profitable manner. As set forth above, Intel’s ability to manufacture the 7 nm process in a timely  
16 fashion was the most critical issue for the Company, its investors, and the value of its stock during the  
17 Class Period. As Intel confirmed in its January 24, 2020 Form 10-K, “Our ability to optimize and apply  
18 our manufacturing expertise to deliver more advanced, differentiated products is *foundational to our*  
19 *current and future success.*” Indeed, for the top executives of one of the world’s most prominent  
20 semiconductor companies to *not* have a detailed understanding of these topics would amount to, at best,  
21 a reckless indifference towards their fundamental job requirements.

22           199. Defendants acknowledged this. As Swan himself confirmed on October 24, 2019,  
23 “improving execution” was one of three “strategic priorities” at the Company and he identified  
24 “manufacturing process node execution” as a critical aspect of that priority. Swan specifically identified  
25 improving yields on 10 nm, “accelerating the pace of process node introductions and moving back to a  
26 2- to 2.5-year cadence,” and being “on track to launch our first 7-nanometer-based product” in 2021 as  
27 examples of the ways Intel was improving its manufacturing process node execution, under his oversight.  
28 Accordingly, given the importance of “manufacturing process node execution” to the Company’s overall

business strategy, the Individual Defendants—three of Intel’s most senior executives—can also be presumed to have knowledge regarding facts adversely impacting its strategy.

200. As Intel’s CEO, Swan was directly responsible for ensuring that the Company’s “strategic priorities” were on track and would therefore have to be informed as to their details in order to track progress against expectations and publicly stated deliverables. Similarly, Defendant Davis also would have been keenly aware of issues regarding the 7 nm process; as Intel’s CFO he regularly spoke publicly about the Company’s Research & Development and Capital Expenditure spending and budgets, as well as the Company’s current and future revenues and margins, all of which hinged directly on the state of Intel’s investment in and progress towards its 7 nm node. Likewise, Defendant Renduchintala was Intel’s chief engineering officer and had direct responsibility over the groups designing and manufacturing Intel’s 7 nm products.

201. Moreover, producing Intel’s most advanced designs outside its own fabs in any meaningful quantity was both antithetical to, and devastating for, its long-held leading-edge IDM model. Because the Company’s IDM model was “foundational to [Intel’s] current and future success,” any decisions to fundamentally alter this structure would be restricted only to Intel’s most senior decision makers. Therefore, accurate information regarding the actual progress of 7 nm and Intel’s likelihood of successful execution would have had to been known and considered among its most senior executives before any such drastic outsourcing step could be initiated. The Individual Defendants were thus intensely focused on progress of the 7 nm node and Intel’s plans to outsource its chip production throughout the Class Period, rendering absurd any suggestion that they were not aware of these critical aspects of the Company’s operations.

**D. The Departure of Key Executives Supports an Inference of Scienter**

202. The departure of several key executives, including Defendants Renduchintala and Swan, from Intel during and after the Class Period is indicative of scienter. Renduchintala was forced from his position as Intel’s most senior engineering officer on July 27, 2020, shortly after the disastrous Q2 2020 earnings call where the 7 nm delays and outsourcing issues were disclosed to the market. Analysts reacted to Renduchintala’s departure as an implicit admission of the dire territory that Intel had entered as a result of the 7 nm delays, particularly given his deep involvement with the Company’s advanced



process node development efforts. For example, one analyst wrote that with “new organizational structure in place and new leadership we would expect only increasing questions over the propensity / need for Intel to turn to external manufacturing partners (e.g., TSMC).”

203. Moreover, Renduchintala’s departure had followed closely on the heels of the abrupt departure of Intel’s highly regarded chip engineer, Keller, announced on June 11, 2020, after a relatively brief stint at the Company. Keller’s close association with several important chip engineering efforts at Intel, including the state of Intel’s manufacturing processes, led to ultimately justified concerns regarding Intel’s competitive positioning and whether Keller had been able to make any impacts within the Company.

204. Likewise, on January 13, 2021, Intel issued a press release announcing that, on February 15, 2021, Swan would step down as Intel’s CEO, thus rendering him the shortest-serving CEO in the Company’s history, by far. Although *The Wall Street Journal* deemed Swan’s “ouster” a “surprise move,” it identified Intel’s “period of technology missteps, market-share losses and pressure from a hedge fund [Third Point LLC]” as precipitating factors.<sup>46</sup> In contrast, Swan’s ouster had come as no surprise to SemiAccurate, which had noted months earlier that “Swan’s departure was a done deal, the timing is more the question,” and that “[g]iven Intel’s dire situation” “we don’t believe [Swan’s] ‘retirement’ is voluntary.”<sup>47</sup>

## VIII. LOSS CAUSATION

205. During the Class Period, as detailed herein, Defendants engaged in a scheme to deceive the market and a course of conduct that artificially inflated the price of Intel common stock and operated as a fraud or deceit on Class Period purchasers of Intel common stock by failing to disclose and misrepresenting the adverse facts detailed herein, including that (1) Intel’s 7 nm launch was not at all “on track”; and (2) one of the “many lessons” coming out of 10 nm was that Intel had been – for the first time in the Company’s history – outsourcing its leading-edge products (i.e., 7 nm) to external foundries. As

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<sup>46</sup> See Asa Fitch, *Intel Ousts CEO Bob Swan*, Wall St. J. (Jan. 13, 2021), <https://www.wsj.com/articles/intel-ceo-bob-swan-steps-down-11610548665>.

<sup>47</sup> See Charlie Demerjian, *Guess who is looking for a new CEO?*, SemiAccurate.com (Oct. 26, 2020), <https://www.semiaccurate.com/2020/10/26/guess-who-is-looking-for-a-new-ceo/>.

1 a result of Defendants' misrepresentations, the price of Intel common stock declined significantly as the  
2 prior artificial inflation came out of the Company's stock price on June 12, July 24, and October 23,  
3 2020. Defendants' misstatements and omissions were the proximate cause of those stock price declines  
4 and the losses suffered by Class members.

5 206. As a result of their purchases of Intel common stock during the Class Period, Lead  
6 Plaintiffs and the other Class members suffered economic loss, i.e., damages, under the federal securities  
7 laws. Defendants' materially false and misleading statements caused Intel common stock to trade at  
8 artificially inflated levels throughout the Class Period, reaching as high as \$69.29 per share on January 24,  
9 2020.

10 207. By concealing from investors the adverse facts detailed herein, Defendants presented a  
11 misleading picture of Intel's business and prospects. As true facts about the Company were revealed to  
12 the market, the price of Intel common stock fell significantly. These declines removed the inflation from  
13 the price of Intel common stock, causing real economic loss to investors who had purchased Intel  
14 common stock during the Class Period.

15 208. The declines in the price of Intel common stock after the corrective disclosures came to  
16 light were a direct result of Defendants' fraudulent misrepresentations being revealed to investors and  
17 the market. The timing and magnitude of the price declines in Intel common stock negate any inference  
18 that the loss suffered by Lead Plaintiffs and the other Class members was caused by changed market  
19 conditions, macroeconomic or industry factors or Company-specific facts unrelated to Defendants'  
20 fraudulent conduct. As one example, on July 23, 2020, despite announcing financial results that  
21 surpassed analysts' expectations, including for revenue and earnings per share, the market reacted  
22 extremely negatively to the news that Intel's 7 nm process would be outsourced and otherwise that the  
23 Company was a year behind the schedule previously represented to the market. As a direct result – and  
24 despite Defendant Davis's touting "record Q2 revenue for CCG, DCG, and memory" during Intel's  
25 July 23, 2020 Q2 earnings call – Intel's stock price declined by \$10.83 per share, or **17.93%**, from a  
26 closing price of \$60.40 per share on July 23, 2020, to a closing price of \$49.57 per share on July 27,  
27 2020.

209. Likewise, on October 22, 2020, Intel announced its Q3 2020 financial results and further disclosed in greater detail that it planned to rely on “external foundry processes” rather than its troubled “Intel 7nm.” The same day, Deutsche Bank analysts wrote that Intel’s “results/guidance . . . were . . . disappointing on key metrics” and that the company had “indicated a decision on internal vs. external manufacturing would be announced in 1Q21 (we’d guess a hybrid approach is adopted)” and lowered their price target for the stock from \$60.00 to \$55.00. The next day, on October 23, 2020, Jefferies analysts noted the conflict between Intel’s previous statements and the Company’s latest revelation regarding outsourcing: “INTC CEO commentary has gone from ‘we continue to look at . . . non-CPU products in foundries’ in January, to ‘our 2023 products will deliver on either Intel 7nm or external foundry processes’ during its Oct ‘20 earnings call.” As a result of these disclosures, Intel’s stock price declined **10.57%**, or \$5.70 per share, from a closing price of \$53.90 per share on October 22, 2020, to a closing price of \$48.20 per share on October 23, 2020.

210. The economic loss, i.e., damages, suffered by Lead Plaintiffs and the other Class members was a direct result of Defendants’ fraudulent scheme to artificially inflate the price of Intel common stock and the subsequent significant decline in the value of Intel common stock when Defendants’ prior misrepresentations and other fraudulent conduct were revealed.

## **IX. APPLICABILITY OF THE PRESUMPTION OF RELIANCE**

211. Lead Plaintiffs and the Class are entitled to a presumption of reliance pursuant to *Basic Inc. v. Levinson*, 485 U.S. 224 (1988), and the fraud-on-the-market doctrine because, during the Class Period, the material misstatements and omissions alleged herein would induce a reasonable investor to misjudge the value of Intel stock and without knowledge of the misrepresented or omitted material facts, Lead Plaintiffs’ funds and other members of the Class purchased or acquired Intel stock between the time Defendants misrepresented and failed to disclose material facts about their business operations and financial prospects, and the time the true facts were disclosed. Accordingly, Lead Plaintiffs’ funds and the other members of the Class relied, and were entitled to have relied, upon the integrity of the market for Intel common stock, and are entitled to a presumption of reliance on Defendants’ materially false and misleading statements during the Class Period.

1           212. At all relevant times, the market for Intel common stock was efficient for the following  
2 reasons, among others:

3                   (a) Intel stock met the requirements for listing, and was listed and actively traded on  
4 the NASDAQ, a highly efficient market;

5                   (b) As a regulated issuer, Intel filed periodic public reports with the SEC; and

6                   (c) Intel regularly communicated with public investors via established market  
7 communication mechanisms, including through regular dissemination of press releases on the major news  
8 wire services and through other wide-ranging public disclosures, such as communications with the  
9 financial press, securities analysts and other similar reporting services.

10           213. Lead Plaintiff and the Class are also entitled to a presumption of reliance under *Affiliated*  
11 *Ute Citizens v. United States*, 406 U.S. 128 (1972), because the claims asserted herein against Defendants  
12 are predicated upon omissions of material fact for which there was a duty to disclose.

13 **X. THE STATUTORY SAFE HARBOR DOES NOT APPLY TO DEFENDANTS’**  
14 **FALSE AND MISLEADING STATEMENTS**

15           214. The statements alleged herein to be materially false and misleading are not subject to the  
16 protections of the PSLRA’s statutory Safe Harbor for forward-looking statements because:

17                   (a) they are not forward looking;  
18                   (b) they are subject to exclusion; or  
19                   (c) even if purportedly forward-looking, Defendants cannot meet the requirements for  
20 invoking the protection, i.e., identifying the statements as forward looking and demonstrating that the  
21 statements were accompanied by meaningful cautionary language.

22           215. Many of the statements were misleading in light of omissions of material present or  
23 historical facts and cannot be considered forward-looking.

24           216. Under the PSLRA’s statutory Safe Harbor for written statements, a forward-looking  
25 statement is protected if it is identified as such and “accompanied by meaningful cautionary language.”  
26 15 U.S.C. § 78u-5(c)(1)(A)(i). An oral forward-looking statement must be accompanied by a cautionary  
27 statement that it is forward-looking, that actual results may differ materially and that additional  
28 information concerning risk factors is contained in a readily available written document. In addition, the

1 oral statement must: (i) identify the written document, or portion thereof, that contains such factors; and  
2 (ii) the referenced written documents must contain meaningful cautionary language. 15 U.S.C. § 78u-  
3 5(c)(2)(B).

4 217. The Safe Harbor excludes from protection all forward-looking statements that are  
5 included in financial statements purportedly prepared in compliance with Generally Accepted  
6 Accounting Principles (“GAAP”), including those filed with the SEC on Form 8-K. 15 U.S.C. § 78u-  
7 5(b)(2)(A).

8 218. Statements of historical fact, current condition or a mixture thereof are not “forward-  
9 looking” and thus not protected by the Safe Harbor.

10 219. Examples of Defendants’ false oral and written statements of current or historical fact  
11 include, but are not limited to:

12 (a) October 24, 2019: “We are on track to launch our first 7-nanometer-based  
13 product, a data center-focused discrete GPU, in 2021, 2 years after the launch of 10-nanometer.”

14 (b) October 24, 2019: Q: “And it sounds like the 7-nanometer GPGPU is still on  
15 track for 2021.” A: “Yes. I mean, first to the comment, yes, the -- nothing new about process relative to  
16 what we said at Analyst Day . . . .”

17 (c) January 23, 2020: “Our 7-nanometer process remains on track to deliver our lead  
18 7-nanometer product, Ponte Vecchio, at the end of 2021, with CPU products following shortly after in  
19 2022.”

20 (d) January 24, 2020: “We are accelerating the pace of process node introductions  
21 and moving back to a 2- to 2.5-year cadence. We are on track to deliver our first 7nm-based product, a  
22 discrete GPU, at the end of 2021.”

23 (e) April 23, 2020: “We indicated that we plan to get back on a 2- to 2.5-year cadence,  
24 which means in 2021, we’ll be ramping 10-nanometer even more while we’re investing in 7-nanometer  
25 that we anticipate having in the fourth quarter of 2021 . . . -- we’re well on track from the plans we laid  
26 out and feel pretty good about a dynamite first quarter and an outlook for the second quarter in line or  
27 better than what we expected.”  
28

1 (f) June 11, 2020: “Looking forward to 7nm, [Intel]’s time-line remains unchanged  
2 with a late 2021 launch.”

3 220. To the extent any of the statements were identified as forward-looking statements, they  
4 do not fall within the protections of the Safe Harbor because they lacked specific, meaningful cautionary  
5 statements identifying important factors that could cause actual results to differ materially from those in  
6 the purportedly forward-looking statements. A warning that identifies a potential risk, but implies that  
7 such a risk had not materialized, i.e., states that something might occur but does not state that something  
8 actually has already occurred, is not meaningful and does not fall within the protections of the Safe  
9 Harbor.

10 221. Meaningful risk disclosures must also be substantive and tailored to the forward-looking  
11 statement they accompany. Many of Defendants’ purported risk disclosures remained unchanged over  
12 the course of the Class Period, despite the fact that such risks had in fact materialized, which change in  
13 circumstance was material to the reasonable investor. Defendants’ risk disclosures were therefore neither  
14 substantive nor tailored and do not satisfy the requirements of the Safe Harbor.

15 222. Indeed, despite representing during the Class Period that “we’re well on track” and “we’re  
16 making good progress” on Intel’s 7 nm product and process, the Company did not update its risk  
17 disclosures concerning “forward-looking statements” to include “statements that refer to . . . our 10nm  
18 and 7nm process technologies” until July 23, 2020, when Intel filed the Form 8-K announcing the  
19 surprising delay (and outsourcing to its competitor) of that same 7 nm process technology. Given that  
20 Intel did not update its “forward-looking statements” risk disclosures to include “7nm” until long after  
21 that very same risk had already transpired, the Company’s risk disclosures on this subject were neither  
22 substantive nor tailored and did not satisfy the requirements of the Safe Harbor.

23 223. Nor were the historic or present-tense statements made by Defendants assumptions  
24 underlying or relating to any plan, projection or statement of future economic performance, as they were  
25 not stated to be such assumptions when made, nor were any of the projections or forecasts made by  
26 Defendants expressly related to or stated to be dependent on those historic or present-tense statements  
27 when made.

224. Defendants' forward-looking statements also do not fall within the protections of the Safe Harbor because they had no reasonable basis. Defendants are liable for those false forward looking statements because, at the time each of those forward-looking statements was made, the particular speaker knew that the particular forward-looking statement was false or misleading and/or the forward-looking statement was authorized and/or approved by an executive officer of Intel, who knew that those statements were false or misleading when made.

## **XI. CONTROL PERSONS**

225. As alleged herein, the Individual Defendants were responsible for drafting, producing, reviewing and/or disseminating the materially false and misleading statements, information and omissions alleged herein; were aware of, or recklessly disregarded, the fact that the false and misleading statements and omissions were being issued by the Company; and approved or ratified these statements, all in violation of the federal securities laws.

226. As officers and controlling persons of a publicly held company whose shares are registered with the SEC and traded on the NASDAQ, the Individual Defendants had a duty to disseminate prompt, accurate and truthful information with respect to Intel and to correct any previously issued statements that had become materially misleading or untrue so that the market price of the Company's common stock would be based upon truthful and accurate information. The Individual Defendants each violated these specific requirements and obligations during the Class Period.

227. The Individual Defendants are liable for disseminating materially false and misleading statements and/or concealing material adverse facts with respect to the Company's progress on its 7 nm node. The Individual Defendants' wrongful course of conduct (i) deceived the investing public regarding the Company's business, operations, management and the intrinsic value of Intel's common stock; (ii) materially misrepresented and omitted to disclose; (iii) caused Lead Plaintiffs' funds and other members of the Class to purchase Intel common stock at artificially inflated prices; and (iv) caused Lead Plaintiffs' funds and other members of the Class to suffer damages when Intel finally disclosed the truth about its 7 nm node failures.

## **XII. CLASS ACTION ALLEGATIONS**

228. Lead Plaintiffs bring this action as a class action pursuant to Rule 23 of the Federal Rules of Civil Procedure on behalf of all persons who purchased or otherwise acquired Intel common stock during the Class Period, i.e., from October 25, 2019 through October 23, 2020, inclusive, and who were damaged thereby (the “Class”). Excluded from the Class are Defendants; members of the immediate families of the Individual Defendants; Intel’s subsidiaries and affiliates; any person who is or was an officer or director of Intel during the Class Period; any entity in which any Defendant has a controlling interest; and the legal representatives, heirs, successors and assigns of any such excluded person or entity.

229. The members of the Class are so numerous that joinder of all members is impracticable. The disposition of their claims in a class action will provide substantial benefits to the parties and the Court. The Company’s stock is actively traded on the NASDAQ and there are more than four billion shares of Intel common stock outstanding. While the exact number of Class members is unknown at this time, and can only be ascertained through appropriate discovery, Lead Plaintiffs believe that there are hundreds or thousands of members in the proposed Class. Record owners and other members of the Class may be identified from records maintained by Intel or its transfer agent and may be notified of the pendency of this action by mail, using the form of notice similar to that customarily used in securities class actions.

230. Common questions of law and fact predominate and include: (i) whether Defendants violated the Exchange Act; (ii) whether Defendants omitted and/or misrepresented material facts; (iii) whether Defendants knew or recklessly disregarded that their statements were false; (iv) whether Defendants’ statements and/or omissions artificially inflated the price of Intel common stock; and (v) the extent and appropriate measure of damages.

231. Lead Plaintiffs’ claims are typical of the claims of the members of the Class, as all members of the Class are similarly affected by Defendants’ wrongful conduct in violation of federal law that is complained of herein.

232. Lead Plaintiffs will fairly and adequately protect the interests of the members of the Class and have retained counsel competent and experienced in class and securities litigation.



233. A class action is superior to all other available methods for the fair and efficient adjudication of this controversy since joinder of all members is impracticable. Furthermore, as the damages suffered by individual Class members may be relatively small, the expense and burden of individual litigation make it impossible for members of the Class to individually redress the wrongs done to them. There will be no difficulty in the management of this action as a class action.

**COUNT I**  
**For Violation of § 10(b) of the Exchange Act And Rule 10b-5**  
**Against All Defendants**

234. Lead Plaintiffs incorporate ¶¶ 1-233 by reference.

235. During the Class Period, Defendants disseminated or approved the false statements specified above, which they knew or recklessly disregarded were materially misleading in that they contained misrepresentations and failed to disclose material facts necessary in order to make the statements made, in light of the circumstances under which they were made, not misleading.

236. Defendants violated § 10(b) of the Exchange Act and Rule 10b-5 in that they:

- (a) Employed devices, schemes, and artifices to defraud;
- (b) Made untrue statements of material fact or omitted to state material facts necessary in order to make the statements made, in light of the circumstances under which they were made, not misleading; or
- (c) Engaged in acts, practices and a course of business that operated as a fraud or deceit upon Lead Plaintiffs' funds and others similarly situated in connection with their purchases of Intel common stock during the Class Period.

237. Lead Plaintiffs' funds and the Class have suffered damages in that, in reliance on the integrity of the market, they paid artificially inflated prices for Intel common stock. Lead Plaintiffs' funds and the Class would not have purchased Intel common stock at the prices they paid, or at all, if they had been aware that the market prices had been artificially and falsely inflated by Defendants' misleading statements.

238. As a direct and proximate result of Defendants' wrongful conduct, Lead Plaintiffs' funds and the other members of the Class suffered damages in connection with their purchases of Intel common stock during the Class Period.

**COUNT II**  
**For Violation of § 20(a) of the Exchange Act**  
**Against the Individual Defendants**

239. Lead Plaintiffs incorporate ¶¶ 1-238 by reference.

240. During the Class Period, the Individual Defendants acted as controlling persons of Intel within the meaning of § 20(a) of the Exchange Act. By virtue of their positions and their power to control public statements about Intel, the Individual Defendants had the power and ability to control the actions of Intel and its employees. Intel violated § 10(b) of the Exchange Act and Rule 10b-5, as set forth above. By reason of such conduct, the Individual Defendants are liable pursuant to § 20(a) of the Exchange Act.

**PRAYER FOR RELIEF**

241. Wherefore, Lead Plaintiffs pray for judgment as follows:

(a) Determining that this action is a proper class action, certifying Lead Plaintiffs as class representatives under Rule 23 of The Federal Rules of Civil Procedure and Lead Plaintiffs' counsel as class counsel;

(b) Awarding Lead Plaintiffs and the members of the class damages and interest;

(c) Awarding Lead Plaintiffs' reasonable costs, including attorneys' fees; and

(d) Awarding such equitable/injunctive or other relief as the court may deem just and proper.

**JURY DEMAND**

242. Lead Plaintiffs demand a trial by jury.

Dated: January 15, 2021

Respectfully submitted,

/s/ Jonathan D. Uslander

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*Counsel for KBC Asset Management NV and SEB  
Investment Management AB and Lead Counsel for the  
Class*

1 **CERTIFICATE OF SERVICE**

2 I hereby certify that on January 15, 2021, I authorized the electronic filing of the foregoing with  
3 the Clerk of the Court using the CM/ECF system which will send notification of such filing to the e-mail  
4 addresses denoted on the attached Electronic Mail Notice List.

5 I certify under penalty of perjury under the laws of the United States of America that the foregoing  
6 is true and correct.

7 Executed on January 15, 2021.

8 /s/ Jonathan D. Uslaner  
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